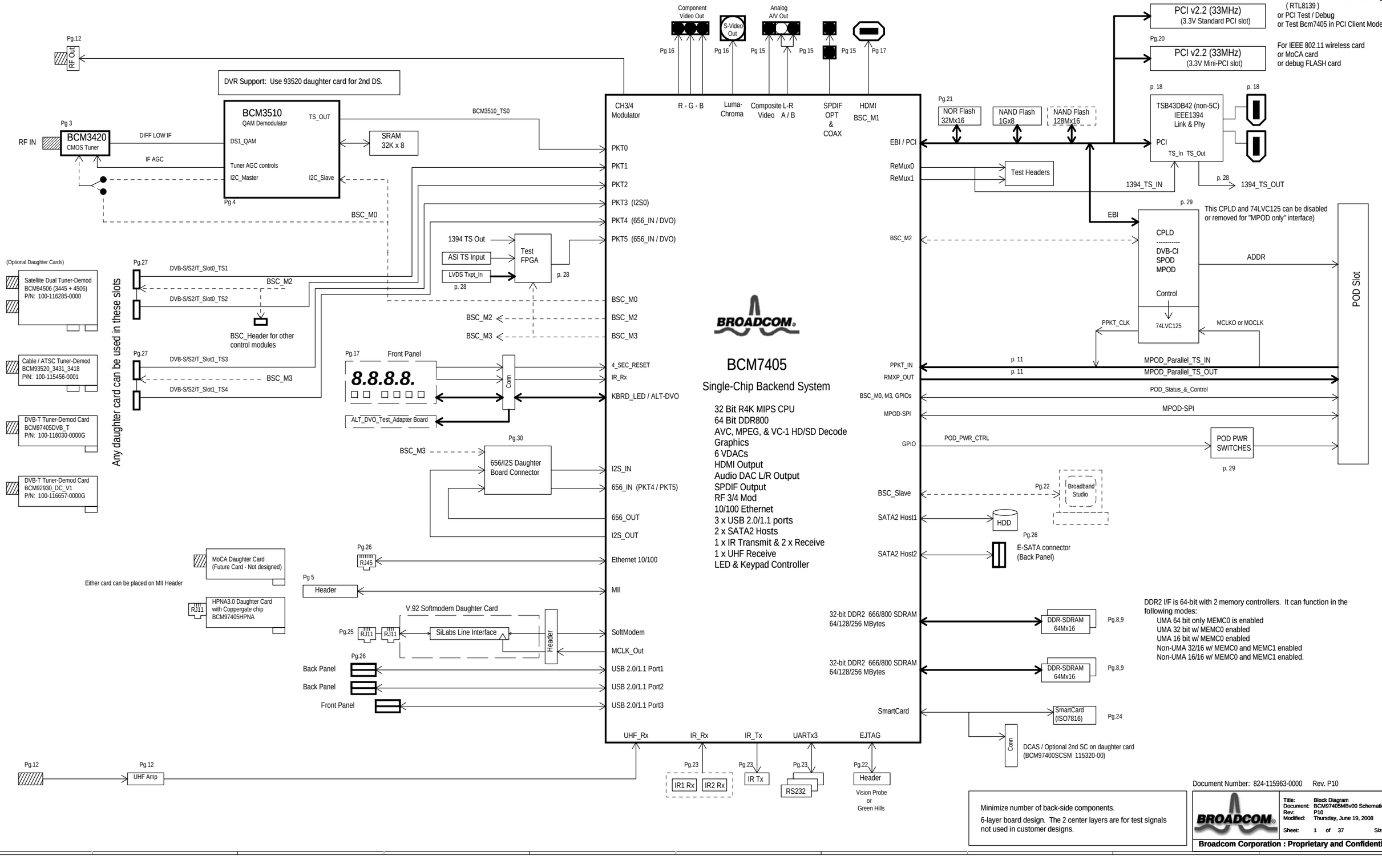
BCM97405 AVC/MPEG/VC-1 HD/SD, Graphics, Digital PVR, IP/Satellite/DVB-C,T Set Top Box



Minimize number of back-side components.

6-layer board design. The 2 center layers are for test signals not used in customer designs.

Document Number: 824-115963-0000 Rev. P10

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ECOs:

ECO BCG-02008: V00 Rev. P1:
- Initial Release

ECO BCG-02042: V00 Rev. P2 changes:
- Pg 28 Changed J1307 to RoHS part.

ECO BCG-02086: V00 Rev. P3 changes:
- Pg 13 Moved RD1306, RD1328 to Position A.
  (Selects correct DRAM size for MEMC0/1)
- Pg 22 Moved RD2201 to Positon B
  (Enables EJTAG.)
- Pg 19 Stuff RN1904, RN1905 with 0 ohms (528499-00)
  (Connect SLOT1 and Transport FPGA to PKT4 and PKT5.)
- Pg 30 Remove RN3001
  (Disconnect PKT5 from I2S output of VDEC-VEC daughter card.)
- Pg 26 Change C2609 to 100pf (500569-00)
  Change R2617 to 4K 1% (502672-00)
  (Correct USB RRef.)

ECO BCG-02114: V00 Rev. P4:
-Agile documentation correction. No impact on schematic.

ECO BCG-02143: V00 Rev. P5:
-Pg 11 Swap SDA and SCL for BSC_M0,2,3 busses
-Pg 13 Replace resistor straps RD1303, RD1304, RD1324 with 3-pin jumpers
  for DDR_Configuration.
-Pg 30 Remove RN3014 and stuff RN3012, RN3013
  with 0 ohm rpacks 528499-00.
  (Enables PKT_VALID[5:0], PKT_ERROR[5:4],
  disables 656 out of J3001:

ECO BCG-02213: V00 Rev. P6:
- New PCB spin. Includes all previous revisions plus:
-Pg 08 Add 20 DDR test pads. Place them close to 7405.
  Move old TP's over by DDR chips.
-Pg 09 Replace Micron DDR2-667 RAM with Samsung DDR2-800
-Pg 11 Swap SDA and SCL for BSC_M1 bus
-Pg 13 Replace resistor straps RD1308, RD1310, RD1322 with 3-pin jumpers
  for Flash/ROM Size1, Flash Type, USB Mode
  Change strapping for CPU frequency to 405 MHz
-Pg 32 Add D5.0V to J216-1 heatsink fan connector.
  Move TP218, TP225 out of POD path. Distribute GND TP's better.
-Pg 37 DNI backup power regulators

ECO CORP-06712: V00 Rev. P7:
-BRCM p/n 502858-00 CAP,CER,0603,0.1uF,20%,16V,X7R) will be made obsolete as it is a duplicate of the BRCM p/n 520192-00. This ECO will update all BOM that currently used 502858-00 and update with 520192-00.

ECO BCG-02417: V00 Rev. P8:
-Pg 03 Change C526, C527 from 1000pf to 27pf. (Fixes slow rise time on BSC_M0.)
-Pg 08 Change R804 to 150 ohms (Fixes RCOMP)
-Pg 21 Replace U2105 with 8Gb NAND Flash
-Pg 22 Change various R and C values in 3OT Crystal circuit.
-Pg 26 Change R2609 from 1k to 1.24k.
  Remove R2605, R2606, R2607, R2608 (E-net PHY already terminated on die)
-Pg 32 Short pins 9, 12 together on U202. (Connects AVIN to PVIN on ER5336QI.)
-Pg 32-33 Corrected Red TP's from 531213-00 to 521741-00.
-Pg 20, 21, 25, 29 Changed 0.1uf caps to 520193-00 to be same as those on Pg 4.
The following changes were made to the schematic:
-Pg 10, 11, etc. Multi-function pin names on Bcm7405 symbol corrected.
-Pg 13 Corrected strapping table:
  "strap_ebi_rom_size" settings for NAND ECC inverted
  "strap_ebi_boot_memory" added info for NAND WR-protect.
-Pg 32, 33 Amperage and Power numbers corrected.
Updated / corrected notes on several pages.

ECO BCG-03062: V00 Rev. P9:
-Pg 04 Change Y601 to 28 MHz (for high-symbol-rate QAM)
-Pg 10 GND RN1025-1,2,3,4 to prevent POD VPP enables from floating.
  Remove RN1026, RN1027 to disconnect UART stubs on MII lines.
  Add 0 ohm to R1016 to connect MII_TX_ERR.
-Pg 10,30 Remove R1022, add jumper to move 3510 IRQ from GPIO_015 to GPIO_024.
-Pg 17 Remove C1708, the 56pf cap on HDMI CEC line.
-Pg 21 Remove R2169 to disable Block Lock on NAND flash.
-Pg 23,24,29 Remove R2301, R2302, R2909 and jumper UART0 Rx/Tx to GPIO_111/112.
  Jumper POD_VCC_ON to GPIO_110.
The following changes were made to the schematic:
-Pg 16 Change 30 MHz filter name to "elliptical".
-Pg 22 Change EJTAG note.
-Pg 24 Add NDS note.
Other minor note changes.

ECO BCG-03757: V00 Rev. P10:
-Pg 08 Change PCOMP, NCOMP terminations (R805, R806) to 24.3 ohms
-Pg 09 Change DDR_CLK terminations to Thevenin (PU/PD)
  Change all VTT terminations to 62 ohms.
The following changes were made to the schematic:
-Pg 08 Revise DDR2 layout rules.
-Pg 26 Add note to use 25-30MHz backup SATA crystal
  Add note to leave E-Net termination pads on board
  Add note to add 1k differential terminations to SATA lines.
-Pg 34 Add note that C114 not needed now that RFM_PLLCAP is just a test port.

Errata:

-Pg 05 Add MICTOR connector to MII lines for logic analyzer.
-Pg 15 Consider using MAX9722 for audio opamps. (for pop suppression)
-Pg 19 Add RMX_PAUSE0/1 to Remux connectors. Stuff DNI'd resistors to enable these paths.
-Pge 21 Add skt footprint for testing various NAND Flash (see Emulation Technology)
-Pg 26 eSATA & E-net ports need ESD protection.
  Add 25-30MHz SATA xtal footprint.
  Change SATA connectors to SMT.
-Pg 32 Split 1.8v power so DDR and 7405 can be measured separately.
  Add GND puddle on Layer 5 under DDR address and data traces on Layer 6.
  Replace Enpirion regulator with another brand.

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NOTES:
1. BCM3420 tuner is an HVQFN40 package with downset paddle.
2. Clear solder mask from all top/bottom GND.
3. Use 1 oz copper.
4. Use the shortest trace for low value capacitors.
5. Make provisions for shielding the entire tuner section.
6. Plated through hole (PTH) vias should be covered by solder mask to prevent molten solder wicking into the vias.

Shield for Tuner

HW500
FENCE_1.00X1.25X0.20

THESE COMPONENTS ARE WITHIN THE SHIELD OUTLINE

Add 36 thermal vias (12 mil diam.) under BCM3420 chip. No solder mask under chip on top and bottom

75 ohm line

CABLE IN

J500 F-TYPE-R/A

C555 150pF

D501 BAV99LT1G

C554 OPEN

L551 1uH (DNI)

ESD scheme dependent

DS_0

U500 BCM3420-A0 HVQFN40_6X6

BCM3420

SILICON CABLE TUNER

NC = 25

FB501 600@100MHz
C501 0.047uF
C502 470pF

FB500 600@100MHz
C503 0.047uF
C504 470pF

FB502 600@100MHz
C510 0.047uF
C512 470pF

C507 4700pF

FB503 600@100MHz
C514 0.047uF
C515 470pF

FB504 600@100MHz
C520 0.047uF
C521 470pF

FB505 600@100MHz
C522 0.047uF
C523 470pF

FB506 600@100MHz
C528 0.047uF
C529 470pF

R501 1K
C505 0.1uF
C506 1000pF
C508 0.1uF
C509 0.1uF

IF0_AGC (4)

Place these parts just outside shield.

100 ohm differential pair

R510 0
C556 DNI
C557 DNI
R511 0

DS0_IF_P (4)
DS0_IF_N (4)

Keep 100 Ohm differential lines short and close to each other.
Width: 5 mils
Spacing: 7 mils
Gap to GND plane: 5.2 mils on layer 1

C516 0.22uF
R505 390
C517 5600pF
R506 180
C518 0.1uF
C519 8200pF

R504 4.7K
R500 4.7K

R509 4.7K

When Bcm3420 selected,
Voltage (AS) = (1k / 5.7k) * VCC ~= 0.18 VCC

(4) RFT_CS_0_TUNER

From 3510

(4) RFT_DATA_TUNER
(4) RFT_CLK_TUNER

From 740x

(4,11) BSC_M0_SCL
(4,11) BSC_M0_SDA

RD501 0
RD502 0

C526 27pF
C527 27pF

R507 56

Short Lines

C524 27pF
C525 27pF

18pF,FUND,4.85X13.3mm
16.000MHz
Y500

PLACE CLOSE TO PINS

Clock Distribution Option:
C524 : 0 ohm
C525 : 15 pF

Bcm3420 I2C Address = 11000[MA1][MA0]x
x = R/W bit
MA1, MA0 are determined by voltage on AS.
See table below:

MA1	*MA0*	*Voltage Applied on AS Input*
0	0	0V to 0.1 x V_{CC}
0	1	Open or 0.2 x V_{CC} to 0.3 x V_{CC}
1	0	0.4 x V_{CC} to 0.6 x V_{CC}
1	1	0.9 x V_{CC} to 1.0 V_{CC}

Therefore in this case, I2C address = 0x61

Cable Tuner XTAL Specifications:
- Fundamental at 16.00 MHz
- Load capacitance: 18.0 pF
- ESR: 50 Ohms Max.
- Tolerance: +/- 50 ppm
- Stability: +/- 100 ppm

3.3V_Tuner

D3.3V
L550 4.7uH
350mA
TP550 RED
+3.3V_TUNER_0
C550 100uF 6.3V
C551 0.1uF
C552 100uF 6.3V
C553 0.1uF

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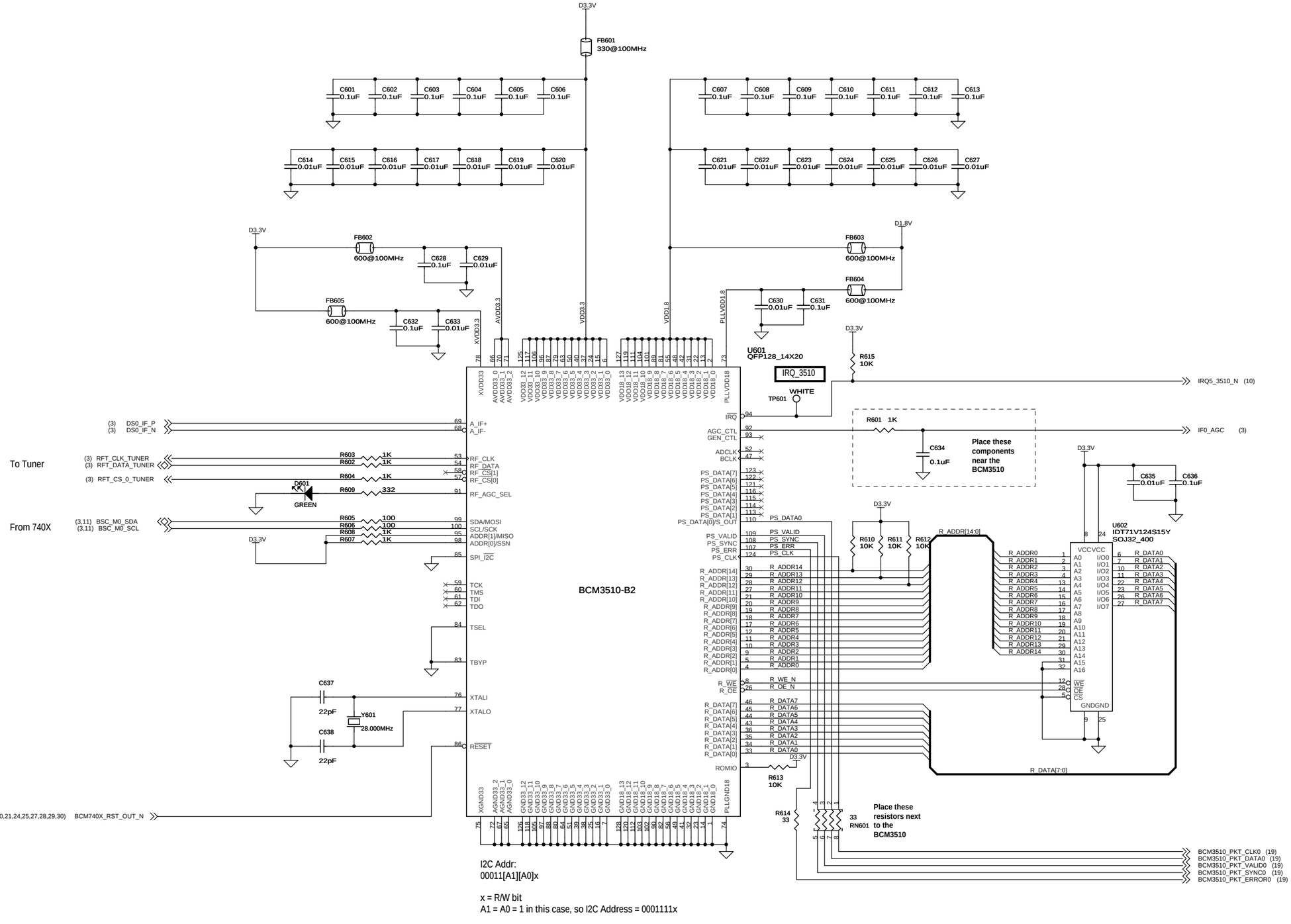

Title:	BCM3510
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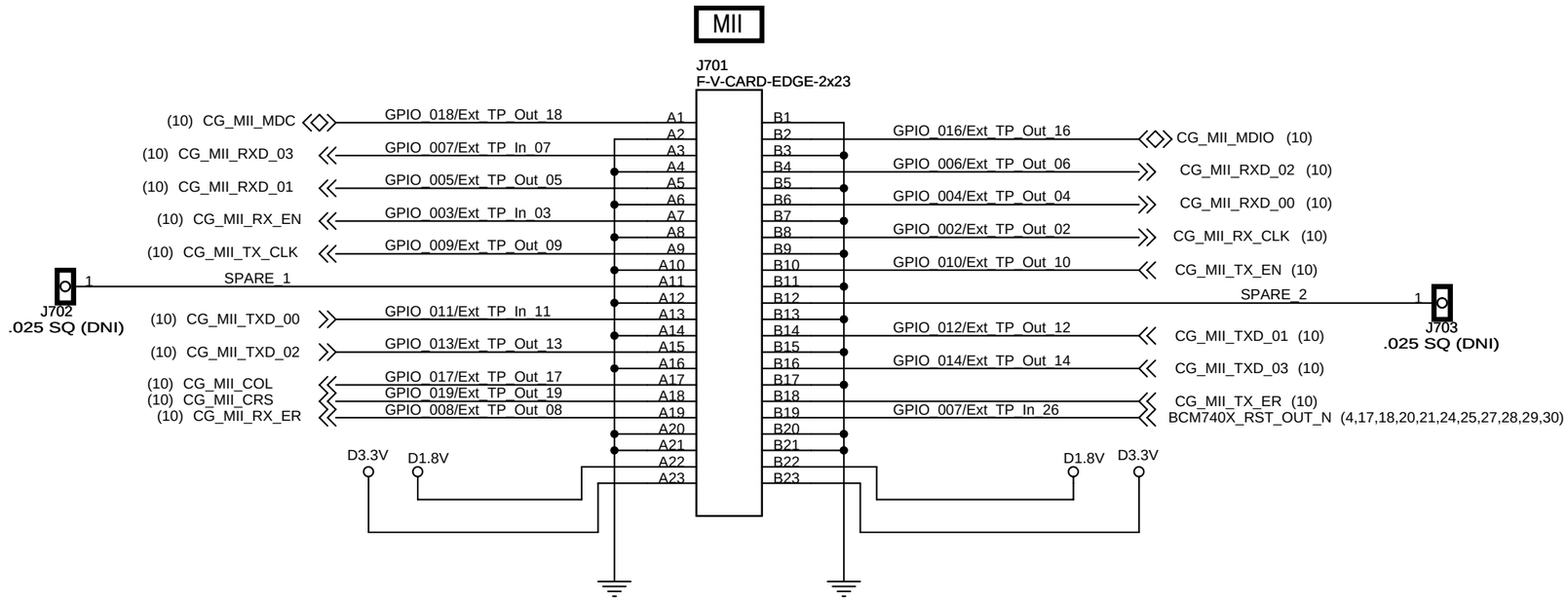

MII Daughter Card Connector for HPNA and MoCA.
Important: Each signal must have an adjacent GND pin.

MII Speed: 50 MHz x 4 lines = 200 Mbits/sec

Add an unplated mounting hole for the daughter card L bracket. Hole size for 4-40 screw.

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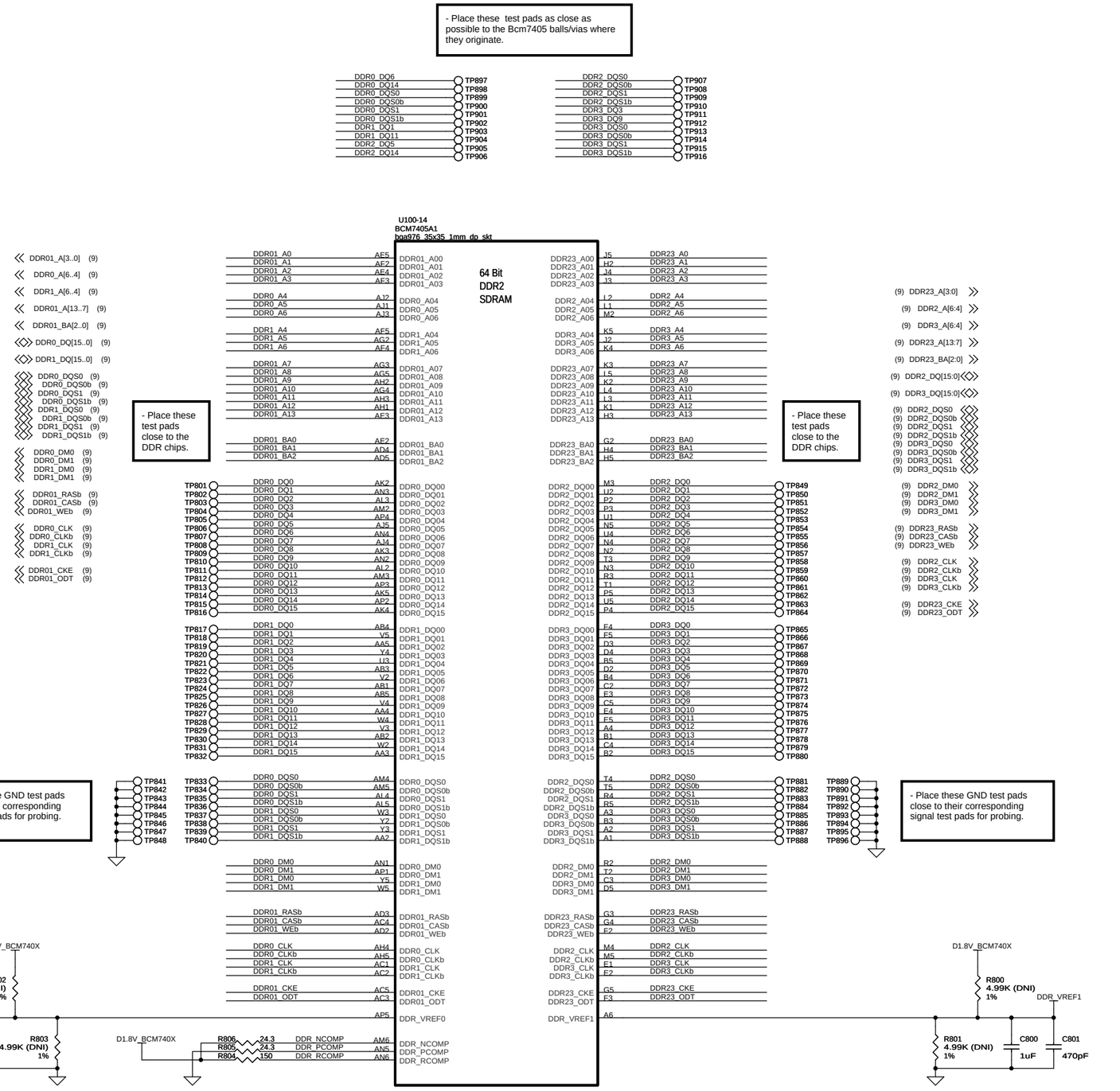

DDR2 rules for 64-bit interface:

BCM7405 pads for DQ / DQS / DM can select ODT impedance of 75 or 150 ohms.

Chip Placement -

Place two DDR2 chips on the top side and two on the bottom, and tuck the DDR2 chips as close to BCM740X DDR2 interface as possible.

Trace lengths -

CLK / CLKb	**< 2" total length, delta in each pair < 50 mils = 1.27mm**
CLK0,1,2,3	**< 50 mils delta among all clocks**
DQS / DQSb	**< 1.5" total length, delta in each pair < 50 mils = 1.27mm**
DQ / DQM	**< 1.5" total length to avoid ISI and crosstalk**
All other	**as short as possible**
DQS / DQ / DM	**< 60ps delta within each byte lane for DDR2-800**
Address / Control	**< 120ps delta with respect to each CLK for DDR2-800**
CLK to DQS	**< 500 mils for the same DDR device (60ps on FR4 = ap. 360 mils = 9mm)**

Trace Impedances -

60 ohms +/- 10% except as noted

CLK / CLKb	**100 ohms +/- 10% differential, 60 ohms +/- 10% single-ended**
DQS / DQSb	**100 ohms +/- 10% differential**

Terminations and Capacitors -

CLK / CLKb -- Place the pull-up / pull-down termination resistors as close to the DDR memory balls as possible. Avoid creating stubs. Route and terminate all 4 CLK's even if not used.

Address / Control -- Place parallel termination resistors/rpacks at end of daisy chains by SDRAM, or if routes are T's then place at branch of T with stubs < 0.200". Termination resistors may be swapped to improve routing.

VREF0 / VREF1 -- Place voltage divider resistors and associated capacitors close to their corresponding balls on the BCM740X chip. Use high-quality ceramic capacitors.

VREF on SDRAM -- Place high-quality ceramic bypass caps close to their corresponding VREF balls as shown on the next sheet of the schematic.

Routing -

DDR_VREF0 and DDR_VREF1: Route as 30 mil trace

Do not tie DDR_VREF to DDR_VTT: It would inject noise onto DDR_VREF.

NCOMP and PCOMP: Route as 10 mil trace

All traces should have >= 3:2 spacing ratio from the reference GND/PWR layer. (e.g. 7.5 mil line-to-line spacing or more for a 5 mil dielectric thickness) It is best if 3:1 ratio is used for DQS / DQ / DM wherever possible.

JEDEC has defined a common landing pattern (CLP) for use with different package options of DDR2 chips. By using the CLP, a PCB can accommodate all DDR2 device configurations and will be compatible with most package options,

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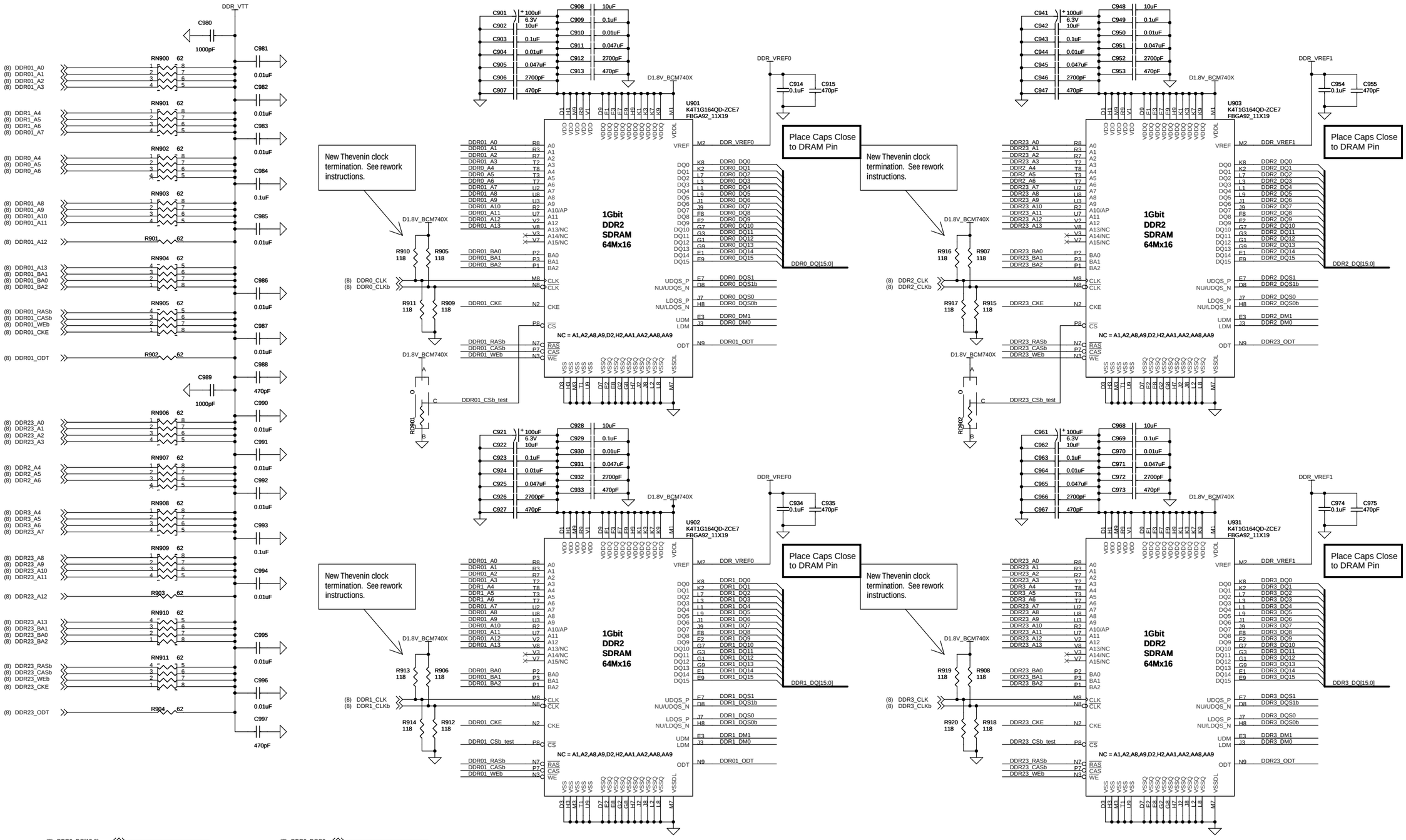

Bcm7405 DDR2 Memory Controller supports up to 1GB memory space of DDR2-800 SDRAM.

This board is laid out to support that, using four 128Mx16 parts (2Gb each).

The BOM currently supplies four 64Mx16 parts of DDR2-800, because the 2Gb parts are extremely expensive.

DDR2 routing rules: See page 8.

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Jumper wires. See P9 Rework Instructions.

(30) IRQ10_3510_N

(4) IRQ5_3510_N — R1022 0 (DNI); RN1025 0 (DNI)

(29) POD_VPP1_EN0
(29) POD_VPP1_EN1
(29) POD_VPP2_EN0
(29) POD_VPP2_EN1

(30) AUD_FS_CLK — R1021 0 (DNI); R1020 0 (DNI)

Place these resistors close to fork to avoid stubs.

(5) CG_MII_MDIO	RN1014	0	GP_MII_MDIO
(5) CG_MII_RXD_03			GP_MII_RXD_03
(5) CG_MII_RXD_02			GP_MII_RXD_02
(5) CG_MII_RXD_01			GP_MII_RXD_01
(5) CG_MII_RXD_00	RN1010	0	GP_MII_RXD_00
(5) CG_MII_RX_EN			GP_MII_RX_EN
(5) CG_MII_RX_CLK			GP_MII_RX_CLK
(5) CG_MII_TX_CLK			GP_MII_TX_CLK
(5) CG_MII_TXD_02	RN1015	0	MII_TXD_02
(5) CG_MII_TXD_03			MII_TXD_03
(5) CG_MII_TXD_00			MII_TXD_00
(5) CG_MII_TXD_01			MII_TXD_01
(5) CG_MII_TX_EN	RN1016	0	MII_TX_EN
(5) CG_MII_CRS			GP_MII_CRS
(5) CG_MII_RX_ER			GP_MII_RX_ER
(5) CG_MII_MDC	R1015	0	MII_MDC
(5) CG_MII_TX_ER	R1016	0	MII_TX_ER
(5) CG_MII_COL	R1019	0	MII_COL

To MII Connector

Place these resistors close to fork to avoid stubs.

CG_MII_RXD_02	RN1020	0 (DNI)	ALT_MII_RXD_02
CG_MII_RXD_03			ALT_MII_RXD_03
CG_MII_MDIO			ALT_MII_MDIO
CG_MII_MDC			ALT_MII_MDC
CG_MII_TX_ER	RN1017	0 (DNI)	ALT_MII_TX_ER
CG_MII_RX_ER			ALT_MII_RX_ER
CG_MII_COL			ALT_MII_COL
CG_MII_TX_EN			ALT_MII_TX_EN
CG_MII_TXD_01	RN1018	0 (DNI)	ALT_MII_TXD_01
CG_MII_TXD_00			ALT_MII_TXD_00
CG_MII_TXD_03			ALT_MII_TXD_03
CG_MII_TXD_02			ALT_MII_TXD_02
CG_MII_TX_CLK	RN1019	0 (DNI)	ALT_MII_TX_CLK
CG_MII_RX_EN			ALT_MII_RX_EN
CG_MII_RXD_00			ALT_MII_RXD_00
CG_MII_RXD_01			ALT_MII_RXD_01
CG_MII_CRS	R1017	0 (DNI)	ALT_MII_CRS

Place these resistors close to Keypad Connector.

ALT_MII_RX_EN	RN1024	0 (DNI)	GPIO_097 (11)
ALT_MII_RXD_00			GPIO_098 (11)
ALT_MII_RXD_01			GPIO_099 (11)
ALT_MII_RXD_02			GPIO_100 (11)
ALT_MII_RXD_03	RN1021	0 (DNI)	GPIO_101 (11)
ALT_MII_RX_ER			GPIO_102 (11)
ALT_MII_TX_CLK			GPIO_086 (11)
ALT_MII_TX_EN			GPIO_087 (11)
ALT_MII_TXD_01	RN1022	0 (DNI)	GPIO_089 (11)
ALT_MII_TXD_00			GPIO_088 (11)
ALT_MII_TXD_03			GPIO_091 (11)
ALT_MII_TXD_02			GPIO_090 (11)
ALT_MII_TX_ER	RN1023	0 (DNI)	GPIO_092 (11)
ALT_MII_MDIO			GPIO_093 (11)
ALT_MII_COL			GPIO_094 (11)
ALT_MII_MDC			GPIO_095 (11)
ALT_MII_CRS	R1018	0 (DNI)	GPIO_096 (11)

Place these resistors close to MII Connector J701 to avoid stubs.

CG_MII_RX_EN	RN1026	0 (DNI)	UART_RXD_0 (23,24)
CG_MII_RXD_00			UART_TXD_0 (23,24)
CG_MII_RXD_01			UART_CTS_0 (23,24)
CG_MII_RXD_02			UART_RTS_0 (23,24)
CG_MII_RXD_03	RN1027	0 (DNI)	UART_RXD_1 (23,24)
CG_MII_RX_ER			UART_TXD_1 (23,24)
CG_MII_TXD_00			UART_RXD_2 (19,23)
CG_MII_TXD_01			UART_TXD_2 (19,23)

To UART Connectors

(31) AGS_TP_IN03	R1023	0 (DNI)	GP_MII_RX_EN
(31) AGS_TP_IN07	R1024	0 (DNI)	GP_MII_RXD_03
(31) AGS_TP_IN11	R1025	0 (DNI)	MII_TXD_00
(31) AGS_TP_IN22	R1026	0 (DNI)	GP_IRQ11_SLOT0A_N
(31) AGS_TP_OUT02	R1027	0 (DNI)	GP_MII_RX_CLK
(31) AGS_TP_OUT04	R1028	0 (DNI)	GP_MII_RXD_00
(31) AGS_TP_OUT05	R1029	0 (DNI)	GP_MII_RXD_01
(31) AGS_TP_OUT06	R1030	0 (DNI)	GP_MII_RXD_02
(31) AGS_TP_OUT08	R1031	0 (DNI)	GP_MII_RX_ER
(31) AGS_TP_OUT09	R1032	0 (DNI)	GP_MII_TX_CLK
(31) AGS_TP_OUT10	R1033	0 (DNI)	MII_TX_EN
(31) AGS_TP_OUT12	R1034	0 (DNI)	MII_TXD_01
(31) AGS_TP_OUT13	R1035	0 (DNI)	MII_TXD_02
(31) AGS_TP_OUT14	R1036	0 (DNI)	MII_TXD_03
(31) AGS_TP_OUT15	R1037	0 (DNI)	MII_TX_ER
(31) AGS_TP_OUT16	R1038	0 (DNI)	GP_MII_MDIO
(31) AGS_TP_OUT17	R1039	0 (DNI)	MII_COL
(31) AGS_TP_OUT18	R1040	0 (DNI)	MII_MDC
(31) AGS_TP_OUT19	R1041	0 (DNI)	GP_MII_CRS
(31) AGS_TP_OUT23	R1042	0 (DNI)	GP_IRQ12_SLOT0B_N

Note: GPIO connections are to the most likely customer destinations.
Place 33 ohm resistors close to 740x.

U100-16
BCM7405A1
bga976_35x35_1mm_dp_skt

GPIO

(26) GP_ENET_ACTIVITY	A16	GPIO_000 / ENET_ACTIVITY / ENET_LINK / Ext. IRQb_13
(26) GP_ENET_LINK	C16	GPIO_001 / ENET_LINK / ENET_ACTIVITY / Ext. IRQb_14
GP_MII_RX_CLK	AB34	GPIO_002 / MII_RX_CLK / Ext. IRQb_0 / EXT_GFX_D9
GP_MII_RX_EN	AB32	GPIO_003 / MII_RX_EN / UART_RXD_0 / EXT_GFX_10 / Ext. IRQb_5
GP_MII_RXD_00	AA34	GPIO_004 / MII_RXD_00 / UART_TXD_0 / EXT_GFX_11 / Ext. IRQb_6
GP_MII_RXD_01	AA33	GPIO_005 / MII_RXD_01 / UART_CTS_0 / EXT_GFX_12 / Ext. IRQb_7 / VEC_HSYNC_0
GP_MII_RXD_02	AA32	GPIO_006 / MII_RXD_02 / UART_RTS_0 / EXT_GFX_13 / Ext. IRQb_8 / VEC_HSYNC_1
GP_MII_RXD_03	Y33	GPIO_007 / MII_RXD_03 / UART_RXD_1 / EXT_GFX_14 / Ext. IRQb_9
GP_MII_RX_ER	Y30	GPIO_008 / MII_RX_ER / UART_TXD_1 / EXT_GFX_15 / Ext. IRQb_10
GP_MII_TX_CLK	AB33	GPIO_009 / MII_TX_CLK / UART_CTS_1 / EXT_GFX_16 / Ext. IRQb_1 / VEC_VSYNC_0
MII_TX_EN — R1000 33 — 33 — GP_MII_TX_EN	W30	GPIO_010 / MII_TX_EN / UART_RTS_1 / EXT_GFX_17 / Ext. IRQb_2 / VEC_VSYNC_1
MII_TXD_01	W32	GPIO_011 / MII_TXD_00 / UART_RXD_2 / EXT_GFX_18 / Ext. IRQb_11
MII_TXD_00	V30	GPIO_012 / MII_TXD_01 / UART_TXD_2 / EXT_GFX_19 / Ext. IRQb_12
MII_TXD_02	W34	GPIO_013 / MII_TXD_02 / UART_CTS_2 / EXT_GFX_20 / TTX0_REQ / Ext. IRQb_3
MII_TXD_03	W33	GPIO_014 / MII_TXD_03 / UART_RTS_2 / EXT_GFX_21 / TTX0_DATA / Ext. IRQb_4
MII_TX_ER — R1001 33	AA31	GPIO_015 / MII_TX_ER / Ext. IRQb_5 / EXT_GFX_22 / RMX_PAUSE0
GP_MII_MDIO	Y32	GPIO_016 / MII_MDIO / Ext. IRQb_6 / EXT_GFX_23 / RMX_PAUSE1
MII_COL — R1008 33	Y31	GPIO_017 / MII_COL / Ext. IRQb_7 / EXT_GFX_VSYNC / AUD_FS_CLK0
MII_MDC — R1007 33	V31	GPIO_018 / MII_MDC / Ext. IRQb_8 / EXT_GFX_25 / AUD_FS_CLK1
GP_MII_CRS	AA30	GPIO_019 / MII_CRS / Ext. IRQb_9 / EXT_GFX_26 / SC_CLK_OUT
(14) GP_IRQ13_SLOT1A_N		
(24,27) IRQ13_SLOT1A_N — R1005 0	V32	GPIO_020 / PWM_0 / Ext. IRQb_13 / SPI_S_SS0b / VEC_VSYNC_0 / SPI_M_SS1b
(14,24) SC_CLK_OUT — R1002 33 — GP_SC_CLK_OUT	U31	GPIO_021 / PWM_1 / Ext. IRQb_14 / SPI_S_MISO / VEC_VSYNC_1 / SC_CLK_OUT
(24,27) IRQ11_SLOT0A_N — R1006 0 — GP_IRQ11_SLOT0A_N	U33	GPIO_022 / IR_INT / Ext. IRQb_11 / UART_RXD_0 / TTX0_REQ / VEC_VSYNC_0
(24,27) IRQ12_SLOT0B_N — R1003 0 — GP_IRQ12_SLOT0B_N	U32	GPIO_023 / IR_IN1 / Ext. IRQb_12 / UART_TXD_0 / TTX0_DATA / VEC_VSYNC_1
(23) IR_IN1 — R1004 0 (DNI)	AD31	GPIO_024 / VI_656_CLK / Ext. IRQb_10
(30) GP_VI_656_CLK — R1009 33 — GP_SPI_M_SCK	L31	GPIO_025 / CHIP2POD_SCLK / SPI_M_SCK / EBI_ADDR_01
(14) SPI_M_SCK	L30	GPIO_026 / POD2CHIP_SDI / SPI_M_MOSI
(14) GP_SPI_M_MOSI	K34	GPIO_027 / CHIP2POD_SDO / SPI_M_MISO / EBI_ADDR_00
(14) GP_SPI_M_MISO	K33	GPIO_028 / CHIP2POD_SCTL / SPI_M_SS0b / EBI_ADDR_02
(14) GP_SPI_M_SS0b	M31	GPIO_029 / POD2CHIP_MISTRT / PPKT_SYNC / PKT_CLK2
(14) GP_PPKT_IN_SYNC		
(14) GP_PPKT_IN_VALID	N30	GPIO_030 / POD2CHIP_MIVAL / PPKT_VALID / PKT_CLK3
(14) GP_PPKT_IN_DATA0	N31	GPIO_031 / POD2CHIP_MDI0 / PPKT_DATA0 / PKT_CLK4
(14) GP_PPKT_IN_DATA1	P30	GPIO_032 / POD2CHIP_MDI1 / PPKT_DATA1 / PKT_DATA2
(14) GP_PPKT_IN_DATA2	L32	GPIO_033 / POD2CHIP_MDI2 / PPKT_DATA2 / PKT_DATA3
(14) GP_PPKT_IN_DATA3	L33	GPIO_034 / POD2CHIP_MDI3 / PPKT_DATA3 / PKT_DATA4
(14) GP_PPKT_IN_DATA4	M32	GPIO_035 / POD2CHIP_MDI4 / PPKT_DATA4 / PKT_SYNC2
(14) GP_PPKT_IN_DATA5	M33	GPIO_036 / POD2CHIP_MDI5 / PPKT_DATA5 / PKT_SYNC3
(14) GP_PPKT_IN_DATA6	M34	GPIO_037 / POD2CHIP_MDI6 / PPKT_DATA6 / PKT_SYNC4
(14) GP_PPKT_IN_DATA7	P31	GPIO_038 / POD2CHIP_MDI7 / PPKT_DATA7 / UART_RXD_2
(14) GP_PPKT_IN_CLK	M30	GPIO_039 / POD2CHIP_MICLK / PPKT_CLK / UART_TXD_2 / EBI_ADDR_13
(14) GP_RMXP_OUT_VALID	T32	GPIO_040 / CHIP2POD_MOVAL / RMXP_VALID / EBI_ADDR_16
(14) GP_RMXP_OUT_SYNC	T33	GPIO_041 / CHIP2POD_MOSTRT / RMXP_SYNC / EBI_ADDR_17
(14) GP_RMXP_OUT_DATA0	R33	GPIO_042 / CHIP2POD_MDO0 / RMXP_DATA0 / EBI_ADDR_18
(24) GP_NDS_SC_AUX0_1	R32	GPIO_043 / CHIP2POD_MDO1 / RMXP_DATA1 / EBI_ADDR_19 / NDS_SC_AUX_0
(24) GP_NDS_SC_AUX1_1	P33	GPIO_044 / CHIP2POD_MDO2 / RMXP_DATA2 / EBI_ADDR_20 / NDS_SC_AUX_1
(24) GP_NDS_SC_VCTRL_1	P32	GPIO_045 / CHIP2POD_MDO3 / RMXP_DATA3 / EBI_ADDR_21 / NDS_SC_VPP
(24) GP_RMXP_OUT_DATA4	N33	GPIO_046 / CHIP2POD_MDO4 / RMXP_DATA4 / EBI_ADDR_22 / SC_IO_1 / CODEC_SDI
(24) GP_RMXP_OUT_DATA5	N34	GPIO_047 / CHIP2POD_MDO5 / RMXP_DATA5 / EBI_ADDR_23 / SC_CLK_1 / CODEC_SCLK
(24) GP_RMXP_OUT_DATA6	N32	GPIO_048 / CHIP2POD_MDO6 / RMXP_DATA6 / EBI_ADDR_24 / SC_RST_1 / CODEC_FSYNCb
(24) GP_RMXP_OUT_DATA7	R31	GPIO_049 / CHIP2POD_MDO7 / RMXP_DATA7 / EBI_ADDR_25 / SC_PRES_1 / CODEC_SDO
(24) GP_RMXP_OUT_CLK	T31	GPIO_050 / CHIP2POD_MOCLK / RMXP_CLK / EBI_ADDR_12 / SC_VCC_1 / CODEC_MCLK
(19) GP_PKT_ERROR0	AD30	GPIO_051 / PKT_ERROR0 / UART_RXD_2 / Ext. IRQb_0 / VI_656_CLK
(19) GP_PKT_ERROR1	AF33	GPIO_052 / PKT_ERROR1 / UART_TXD_2 / Ext. IRQb_1 / EXT_GFX_EN
(19,29) GP_PKT_ERROR2	AF31	GPIO_053 / PKT_ERROR2 / UART_CTS_2 / Ext. IRQb_2 / POD2CHIP_MCLKI / EBI_ADDR_14
(19,29) GP_PKT_ERROR3	AG31	GPIO_054 / PKT_ERROR3 / UART_RTS_2 / Ext. IRQb_3 / CHIP2POD_MCLKO / EBI_ADDR_15
(30) GP_VI_656_D0	AC32	GPIO_055 / PKT_ERROR4 / VI_656_0 / UART_RXD_0
(30) GP_VI_656_D1	AC33	GPIO_056 / PKT_ERROR5 / VI_656_1 / UART_TXD_0 / I2S_LR1_OUT / I2S_LR0_IN
(30) GP_VI_656_D2	AD32	GPIO_057 / PKT_VALID0 / VI_656_2 / UART_CTS_0 / Ext. IRQb_5 / TTX0_REQ
(30) GP_VI_656_D3	AD33	GPIO_058 / PKT_VALID1 / VI_656_3 / UART_RTS_0 / Ext. IRQb_6 / TTX0_DATA
(30) GP_VI_656_D4	AB31	GPIO_059 / PKT_VALID2 / VI_656_4 / UART_CTS_1 / Ext. IRQb_7 / VEC_VSYNC_0
(30) GP_VI_656_D5	AB30	GPIO_060 / PKT_VALID3 / VI_656_5 / UART_RTS_1 / Ext. IRQb_8 / VEC_VSYNC_1
(30) GP_VI_656_D6	AC31	GPIO_061 / PKT_VALID4 / VI_656_6 / UART_RXD_1 / I2S_CLK1_OUT / I2S_CLK0_IN
(30) GP_VI_656_D7	AC30	GPIO_062 / PKT_VALID5 / VI_656_7 / UART_TXD_1 / I2S_DATA1_OUT / I2S_DATA0_IN

D3.3V — R3769 1K

J1000

GP_MII_TX_ER	GPIO_015/Ext_TP_Out_15	1
GP_IRQ11_SLOT0A_N	GPIO_022/Ext_TP_In_22	2
GP_IRQ12_SLOT0B_N	GPIO_023/Ext_TP_Out_23	3

S-M-.100-1X3

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U100-23
BCM7405A1
bga976_35x35_1mm_dp_skt

Reserved Pins

RSV_1 R30
RSV_2 T30
RSV_3 AG30

bga976_35x35_1mm_dp_skt

To Keypad Connector

RN3200 0

(17) FP_LED_LS_0 4 5 GPIO_090
(17) FP_LED_LS_1 3 6 GPIO_091
(17) FP_LED_LS_2 2 7 GPIO_092
RN3201 1 8 0
(17) FP_LED_LS_3 4 5 GPIO_093
(17) FP_LED_LS_4 3 6 GPIO_094
(17) FP_LED_KD_0 2 7 GPIO_086
(17) FP_LED_KD_1 1 8 0 GPIO_087
RN3202
(17) FP_LED_KD_2 4 5 GPIO_088
(17) FP_LED_KD_3 3 6 GPIO_089
(17) FP_LED_LD_0 2 7 GPIO_095
(17) FP_LED_LD_1 1 8 0 GPIO_096
RN3203
(17) FP_LED_LD_2 4 5 GPIO_097
(17) FP_LED_LD_3 3 6 GPIO_098
(17) FP_LED_LD_4 2 7 GPIO_099
(17) FP_LED_LD_5 1 8 GPIO_100
(17) FP_LED_LD_6 R3200 0 GPIO_101
(17) FP_LED_LD_7 GPIO_102

U100-22
BCM7405A1
bga976_35x35_1mm_dp_skt

GPIO

(19) GP_PKT_CLK0 AE32 GPIO_063 / PKT_CLK0
(19) GP_PKT_CLK1 AG34 GPIO_064 / PKT_CLK1

(19) GP_PKT_CLK2 AE30 GPIO_065 / PKT_CLK2 / EXT_GFX_27
(19) GP_PKT_CLK3 AH33 GPIO_066 / PKT_CLK3 / EXT_GFX_28
(19) GP_PKT_CLK4 AJ33 GPIO_067 / PKT_CLK4 / EXT_GFX_29 / VI_656_0 / UART_RXD_2
(19,30) GP_PKT_CLK5 AJ30 GPIO_068 / PKT_CLK5 / I2S_CLK0_IN / VI_656_1 / UART_TXD_2 / I2S_CLK0_OUT
(19) GP_PKT_DATA0 AE32 GPIO_069 / PKT_DATA0

(19) GP_PKT_DATA1 AG32 GPIO_070 / PKT_DATA1
(19) GP_PKT_DATA2 AE30 GPIO_071 / PKT_DATA2 / EXT_GFX_30
(19) GP_PKT_DATA3 AH32 GPIO_072 / PKT_DATA3 / EXT_GFX_31
(19) GP_PKT_DATA4 AH31 GPIO_073 / PKT_DATA4 / EXT_GFX_IN_CLK / VI_656_2 / UART_CTS_2
(19,30) GP_PKT_DATA5 AH30 GPIO_074 / PKT_DATA5 / I2S_DATA0_IN / VI_656_3 / UART_RTS_2 / I2S_DATA0_OUT

(19) GP_PKT_SYNC0 AE33 GPIO_075 / PKT_SYNC0
(19) GP_PKT_SYNC1 AG33 GPIO_076 / PKT_SYNC1
(19) GP_PKT_SYNC2 AF31 GPIO_077 / PKT_SYNC2 / EXT_GFX_24
(19) GP_PKT_SYNC3 AH34 GPIO_078 / PKT_SYNC3 / EXT_GFX_HSYNC
(19) GP_PKT_SYNC4 AJ32 GPIO_079 / PKT_SYNC4 / EXT_GFX_OUT_CLK / VI_656_4 / UART_RXD_0

(19,30) GP_PKT_SYNC5 AJ31 GPIO_080 / PKT_SYNC5 / I2S_LR0_IN / VI_656_5 / UART_TXD_0 / I2S_LR0_OUT
(24) GP_SC_IO_1 AK13 GPIO_081 / SC_IO_1 / NDS_SC_IO / Ext. IRQb_0
(24) GP_SC_CLK_1 AN14 GPIO_082 / SC_CLK_1 / NDS_SC_CLK / Ext. IRQb_1 / UART_RXD_1
(24) GP_SC_RST_1 AM14 GPIO_083 / SC_RST_1 / NDS_SC_RST / Ext. IRQb_2 / UART_TXD_1
(24) GP_SC_PRES_1 AP6 GPIO_084 / SC_PRES_1 / NDS_SC_PRES / Ext. IRQb_3 / UART_CTS_1

(24) GP_SC_VCC_1 AP14 GPIO_085 / SC_VCC_1 / NDS_SC_VCC / Ext. IRQb_4 / UART_RTS_1
(10) GPIO_086 GPIO_086 AL11 GPIO_086 / LED_KD_0 / MII_TX_CLK / DVO0_DE
(10) GPIO_087 GPIO_087 AK11 GPIO_087 / LED_KD_1 / MII_TX_EN / DVO0_CLK_N
(10) GPIO_088 GPIO_088 AL10 GPIO_088 / LED_KD_2 / MII_TXD_00 / DVO0_00
(10) GPIO_089 GPIO_089 AK10 GPIO_089 / LED_KD_3 / MII_TXD_01 / DVO0_01

(10) GPIO_090 GPIO_090 AM11 GPIO_090 / LED_LS_0 / MII_TXD_02 / DVO0_02
(10) GPIO_091 GPIO_091 AN11 GPIO_091 / LED_LS_1 / MII_TXD_03 / DVO0_03
(10) GPIO_092 GPIO_092 AP11 GPIO_092 / LED_LS_2 / MII_TX_ER / DVO0_VSYNC
(10) GPIO_093 GPIO_093 AL12 GPIO_093 / LED_LS_3 / MII_MDIO / DVO0_HSYNC
(10) GPIO_094 GPIO_094 AK12 GPIO_094 / LED_LS_4 / MII_COL / DVO0_04

(10) GPIO_095 GPIO_095 AL9 GPIO_095 / LED_LD_0 / MII_MDC / DVO0_05
(10) GPIO_096 GPIO_096 AK9 GPIO_096 / LED_LD_1 / MII_CRS / DVO0_06
(10) GPIO_097 GPIO_097 AM7 GPIO_097 / LED_LD_2 / MII_RX_EN / DVO0_07
(10) GPIO_098 GPIO_098 AL8 GPIO_098 / LED_LD_3 / MII_RXD_00 / DVO0_08
(10) GPIO_099 GPIO_099 AK8 GPIO_099 / LED_LD_4 / MII_RXD_01 / DVO0_09

(10) GPIO_100 GPIO_100 AL7 GPIO_100 / LED_LD_5 / MII_RXD_02 / DVO0_10
(10) GPIO_101 GPIO_101 AK7 GPIO_101 / LED_LD_6 / MII_RXD_03 / DVO0_11
(10) GPIO_102 GPIO_102 AN8 GPIO_102 / LED_LD_7 / MII_RX_ER / DVO0_CLK_P
(24) GP_SC_EXT_CLK AM9 GPIO_103 / SC_EXT_CLK
(24) GP_SC_IO_0 AN9 GPIO_104 / SC_IO_0 / NDS_SC_IO / Ext. IRQb_0 / UART_RXD_0

(24) GP_SC_CLK_0 AM8 GPIO_105 / SC_CLK_0 / NDS_SC_CLK / Ext. IRQb_1 / UART_TXD_0
(24) GP_SC_RST_0 AM10 GPIO_106 / SC_RST_0 / NDS_SC_RST / Ext. IRQb_2 / UART_CTS_0
(24) GP_SC_PRES_0 AP10 GPIO_107 / SC_PRES_0 / NDS_SC_PRES / Ext. IRQb_9 / UART_RTS_0
(24) GP_SC_VCC_0 AN10 GPIO_108 / SC_VCC_0 / NDS_SC_VCC / Ext. IRQb_10
(24) GP_NDS_SC_AUX0_2 E8 GPIO_109 / CODEC_SDI / Ext. IRQb_11 / UART_CTS_0 / SPI_M_SCK / NDS_SC_AUX_0

(24) GP_NDS_SC_AUX1_2 D8 GPIO_110 / CODEC_SCLK / Ext. IRQb_12 / UART_RTS_0 / SPI_M_MOSI / NDS_SC_AUX_1
(24) GP_NDS_SC_VCTRL_2 E9 GPIO_111 / CODEC_FSYNCb / Ext. IRQb_13 / UART_RXD_0 / SPI_M_MISO / NDS_SC_VPP
(29) GP_POD_VCC_ON D9 GPIO_112 / CODEC_MCLK / Ext. IRQb_14 / UART_TXD_0 / SPI_M_SS0b

D3.3V
C3200
0.01uF
R3212 2.7K
R3217 2.7K
R3218 2.7K
R3219 2.7K
R3229 2.7K
R3233 2.7K
C3201
0.01uF

Optional noise rejection LPF to minimize noise to tuner

R3211 0
R3213 0
R3215 0
R3214 0
R3220 0
R3216 0

(3,4) BSC_M0_SCL
(3,4) BSC_M0_SDA
(17) GP_BSC_M1_SCL
(17) GP_BSC_M1_SDA
(27,29) BSC_M2_SCL
(27,29) BSC_M2_SDA
(27,28,30) BSC_M3_SCL
(27,28,30) BSC_M3_SDA

GP_BSC_M0_SCL U30
GP_BSC_M0_SDA V31
B16
D17
GP_BSC_M2_SCL V33
GP_BSC_M2_SDA V34
GP_BSC_M3_SCL AM12
GP_BSC_M3_SDA AN12

SGPIO_00 / BSC_M0_SCL
SGPIO_01 / BSC_M0_SDA
SGPIO_02 / BSC_M1_SCL
SGPIO_03 / BSC_M1_SDA
SGPIO_04 / BSC_M2_SCL
SGPIO_05 / BSC_M2_SDA
SGPIO_06 / BSC_M3_SCL
SGPIO_07 / BSC_M3_SDA

C3202 18pF (DNI)
C3203 18pF (DNI)
C3204 18pF (DNI)
C3205 18pF (DNI)
C3206 18pF (DNI)
C3207 18pF (DNI)

D3.3V RD1401 D5.0V
0 (DNI)
B A C
C1409 10uF 6.3V
J1402 S-M-.100-1X4 (DNI)
SGPIO_00 1
SGPIO_01 2
3
4
BSC_M0

D3.3V RD1402 D5.0V
0 (DNI)
B A C
C1410 10uF 6.3V
J1403 S-M-.100-1X4 (DNI)
SGPIO_04 1
SGPIO_05 2
3
4
BSC_M2

D3.3V RD1403 D5.0V
0 (DNI)
B A C
C1413 10uF 6.3V
J1404 S-M-.100-1X4 (DNI)
SGPIO_06 1
SGPIO_07 2
3
4
BSC_M3

IRQ's used in this design:

02 -- ITU-BR 656
03 -- POD
10 -- Bcm3510
11 -- Slot 0A
12 -- Slot 0B
13 -- Slot 1A
14 -- Slot 1B

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LNA Center Frequency Options:

Frequency	L1202
433 MHz	1.6 nH
385 MHz	2.7 nH

D5.0V
FB1201
600@100MHz
500mA,300mOHM
C1210 10uF 6.3V
C1226 470pF
C1227 47pF
L1202 1.6nH
R1202 66.5
R1231 82
R1234 24.9K
R1233 51K
C1229 470pF
Q1202 BFR181
Q1201 BFR181
CD1201 470pF INSTALL POSITION A
CD1202 470pF INSTALL POSITION A
T1201 617DB-1024 (DNI)
R1232 215 (DNI)
J1202 SMA-STR (DNI)

UHF Receiver
Antenna Connector
J1201 F-TYPE-R/A
D1201 BAV99LT1G (DNI)
C1211 DNI
L1204 DNI
L1203 12nH
C1228 470pF
ESD scheme dependent

The LNA area uses a 2-layer PCB, but the long traces from CD1201/CD1202 to BCM740x uses 4-layer. Copy the LNA component pads, floods, and vias exactly the same as the Broadcom's reference layout.

Route as 50 Ohm differential references to layer 2 (7 mils width), separate differential traces by at least 12 mils.

U100-13
BCM7405A1
bga976_35x35_1mm_dp_skt
Analog I/O
DIFF_UHF_IN_P A31 UHF_IN_P
DIFF_UHF_IN_N A30 UHF_IN_N
UHF_IFI A32 UHF_IFI0
UHF_IFO B32 UHF_IFO0
UHF_RXTEST F29 UHF_RXTEST TP1201
RFM_PLL_TEST G25
RFM_EXT_R_POS B28
RFM_EXT_R_NEG A28
RFMOUT_P B27
RFMOUT_N A27

IF Filter
C1230 0.01uF
FL1201 10.70MHz
R1235 332
J1203 SMA-STR (DNI)

A2.5V_BCM740X
R1201 0
C1201 220uF 4V
C1202 0.1uF
C1203 1000pF

TP1202
R1210 6.04K 1%
Do NOT connect RFM_EXT_R_NEG to ground.

R1205 75
R1211 75
Place termination resistors next to balls on BCM7400.

Route RFM_DAC_P and RFM_DAC_N as 150 Ohm differential pair, reference to V_CENTER plane on layer 3.

C1225 DNI
T1202 #458PT-1566
RFM_DAC_P
V_CENTER
RFM_DAC_N

3 Pole Chebyshev LPF
Fc ~ 100 MHz
ZI=75 Z0 = 75
L1201 180nH
C1207 33pF
C1208 33pF

Divider
or
Pi Pad Placeholder
R1206 510
R1208 82
R1209 82

Use 75 Ohm line all the way to F-connector J1204.

CH3_4_RF_OUT
C1209 1000pF
J1204 F-TYPE-R/A
CH3/4
RF-Out to TV

Place all circuits from transformer T1202 to C1209 near F-connector J1204.

R1230 0 (DNI)
R1229 0 (DNI)
Place R1229/R1230 near T1202 to minimize the stubs from RFM output.
R1228 0 (DNI)
Place R1228 near R1206 to minimize the stubs from RFM output.

RF Output Level Options:

Approximate RF Output Level	R1208 R1209 (5%)	R1206 (5%)
+40 dBmV	430 Ohm	27 Ohm
+30 dBmV	110 Ohm	180 Ohm
+20 dBmV (Default)	82 Ohm	510 Ohm
+15 dBmV	82 Ohm	1000 Ohm
+10 dBmV	82 Ohm	1800 Ohm
0 dBmV	75 Ohm	5600 Ohm

A5.0V
R1236 1K
C1232 DNI
R1237 1K
R1238 0
C1234 DNI
R1240 1K
R1241 0
C1235 DNI
R1243 1K
U1201A NJM4580V SSOP8
C1231 0.1uF
R1239 100
C1233 100uF
R1242 DNI
C1236 0.1uF
A-5.0V

This portion of circuits is the test circuit for BTSC audio.
The output drives the audio input of an external RFM.

A5.0V
U1201B NJM4580V SSOP8
A-5.0V

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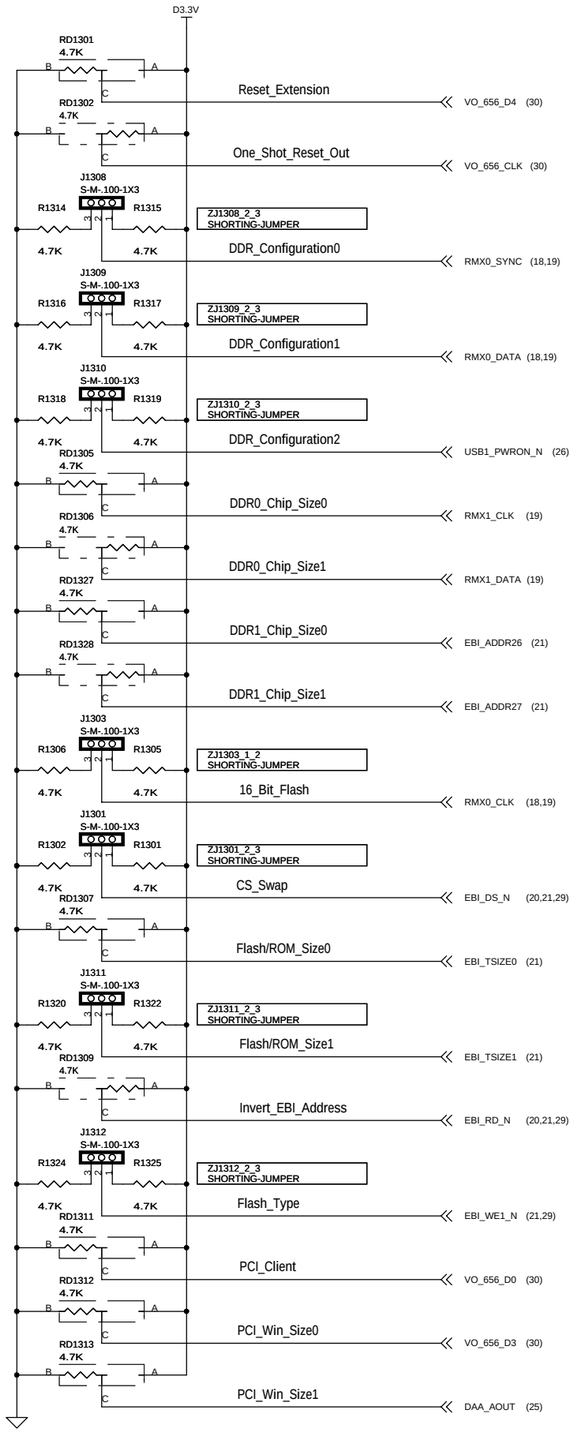
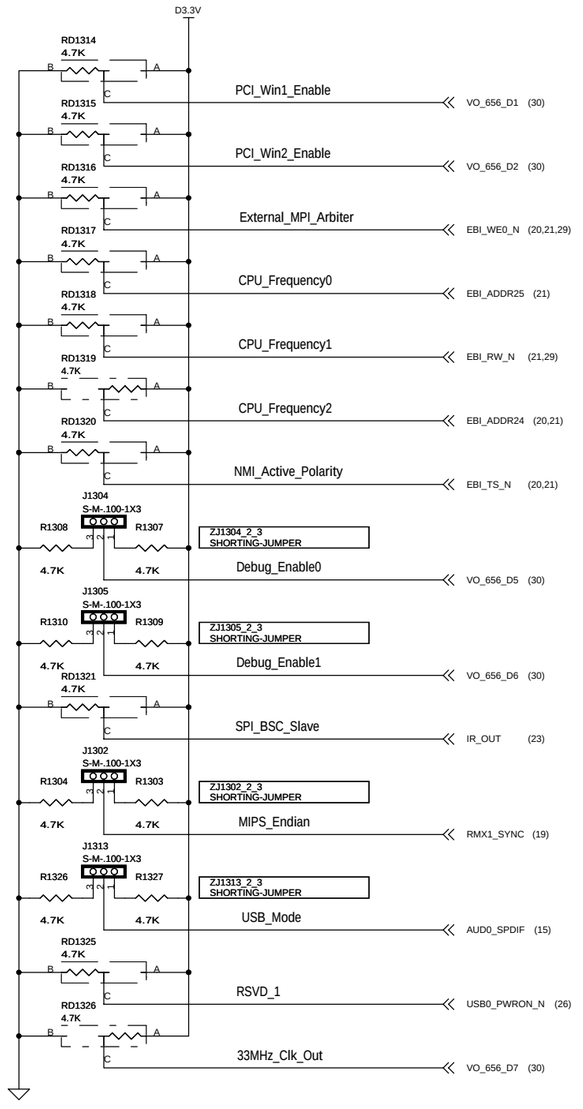
Broadcom Corporation : Proprietary and Confidential

BCM7405Ax Strap Options

Strap Name	Strap Bit	Description	Pin	Default	Comments
Reset_Extension	strap_reset_ext_mode	0: No delay 1: 200 ms (EBI_CS# delayed by 1.6 ms)	VO_656_4	0	
One_Shot_Reset_Out	strap_reset_outb_def_val	0: Level reset output behavior 1: One shot reset output behavior	VO_656_CLK	1	One shot reset output behavior is compatible to BCM3560
DDR_Configuration[2:0]	strap_ddr_config_0 strap_ddr_config_1 strap_ddr_config_2 (LSB is 0, MSB is 2)	000: 64-bit UMA (MEMC0) 001: 32-bit UMA (MEMC0) 010: 16-bit UMA (MEMC0) 100: 32 +16 Non-UMA (MEMC0:32-bit, MEMC1:16-bit) 101: 16 +16 Non-UMA (MEMC0:16-bit, MEMC1:16-bit) (LSB is 0, MSB is 2)	RMX_SYNC0 RMX_DATA0 USB1_PWRON	0 0 0	Configuration of 64-bit DDR interface Currently, 32-bit UMA is NOT supported by 7405.
DDR0_Chip_Size[1:0]	strap_ddr0_device_config_0 strap_ddr0_device_config_1	00: 16Mx16 bit devices on MEMC0 01: 32Mx16 bit devices on MEMC0 10: 64Mx16 bit devices on MEMC0 11: 128Mx16 bit devices on MEMC0	RMX_CLK1 RMX_DATA1	0 1	Device configuration of MEMC0
DDR1_Chip_Size[1:0]	strap_ddr1_device_config_0 strap_ddr1_device_config_1	00: 16Mx16 bit device on MEMC1 01: 32Mx16 bit device on MEMC1 10: 64Mx16 bit device on MEMC1 11: 128Mx16 bit device on MEMC1	EBI_ADDR26 EBI_ADDR27	0 1	Device configuration of MEMC1 (32 + 16 bit mode)
16_Bit_Flash	strap_ebi_boot_memory	If strapped for NOR boot: 0: Boot memory is 8-bit device 1: Boot memory is 16-bit device If strapped for NAND boot: 0: NAND Block 0 not WR-protected 1: NAND Block 0 is WR-protected	RMX_CLK0	?	Per system configuration
CS_Swap	strap_ebi_cs_swap	0: No swap 1: Swap CS_0 and CS_1 signals	EBI_DSb	?	Per system configuration
Flash/ROM_Size[1:0]	strap_ebi_rom_size0 strap_ebi_rom_size1	NOR Flash 0: 64 Mbyte ROM 1: 16 Mbyte ROM 2: 8 Mbyte ROM 3: 4 Mbyte ROM (LSB is 0, MSB is 1) NAND Flash 0: Disable ECC 1: Disable ECC 2: Enable ECC 3: Enable ECC	EBI_TSIZE0b EBI_TSIZE1b	? ?	Per system configuration
Invert_EBI_Address	strap_ebi_invert_addr	0: Do not invert EBI address 1: Invert upper bits of EBI address	EBI_RDb	1	Tom thinks it's more desirable to have the default be "Invert upper bits of EBI address".
Flash_Type	strap_boot_rom_type	0: Boot ROM is NOR Flash 1: Boot ROM is NAND Flash	EBI_WE1b	?	TBD
PCI_Client	strap_pci_client	0: PCI in bridge (master) mode 1: PCI in client (slave) mode	VO_656_0	0	Usually in master mode
PCI_Win_Size[1:0]	strap_pci_memwin_size_0 strap_pci_memwin_size_1	0: 512 Mbyte Window 1: 1 Gbyte Window 2: 128 Mbyte Window 3: 256 Mbyte Window (LSB is 0, MSB is 1)	VO_656_3 DAA_AOUT	?	Per memory configuration
PCI_Win1_Enable	strap_pci_memwin1_en	0: Disable PCI memory window 1 1: Enable PCI memory window 1	VO_656_1	?	Per system configuration
PCI_Win2_Enable	strap_pci_memwin2_en	0: Disable PCI memory window 2 1: Enable PCI memory window 2	VO_656_2	?	Per system configuration
External_MPI_Arbiter	strap_external_MPI_arbit	0: Use internal MPI arbiter 1: Use external MPI arbiter	EBI_WE0b	0	Per system configuration
CPU_Frequency[2:0]	strap_CPU_freq_0 strap_CPU_freq_1 strap_CPU_freq_2	0: 297 MHz 1: 324 MHz 2: 351 MHz 3: 378 MHz 4: 405 MHz (default) 5: 432 MHz 6: 459 MHz 7: 148.5 MHz (297 divided by 2)	EBI_ADDR25 EBI_RWb EBI_ADDR24	0 0 ?	Per system configuration 3'b010 is the recommended default.
NMI_Active_Polarity	strap_NMI_polarity	0: Low-active interrupt 1: High-active interrupt	EBI_TSb	?	Per system configuration
Debug_Enable[1:0]	strap_test_debug_en_0 strap_test_debug_en_1	0: Debug mode disabled	VO_656_5 VO_656_6	0 0	Internal Debug Port
SPI_BSC_Slave	strap_spi_slave_enable	0: BSC slave port configured 1: SPI slave port configured	IR_OUT	0	Per system configuration - usually in BSC slave
MIPS_Endian	strap_system_big_endian	0: System is LITTLE endian 1: System is BIG endian	RMX_SYNC1	?	Per system configuration
USB_Mode	strap_USB_mode	0: 3rd USB is host mode 1: 3rd USB is client mode	AUD0_SPDIF	0	Per system configuration
RSVD_1	strap_RSVD_1	TBD	USB0_PWRON	0	Per system configuration
33MHz_Clk_Out	strap_33_27_MHz_clock	0: 27 MHz clock output 1: 33 MHz clock output	VO_656_7	1	Per system configuration





Circuits connected to these strapping signals such as EBI, RMX , VO, etc. must not affect the strapping, in some cases, buffers are needed.

Title:	Pin Strapping
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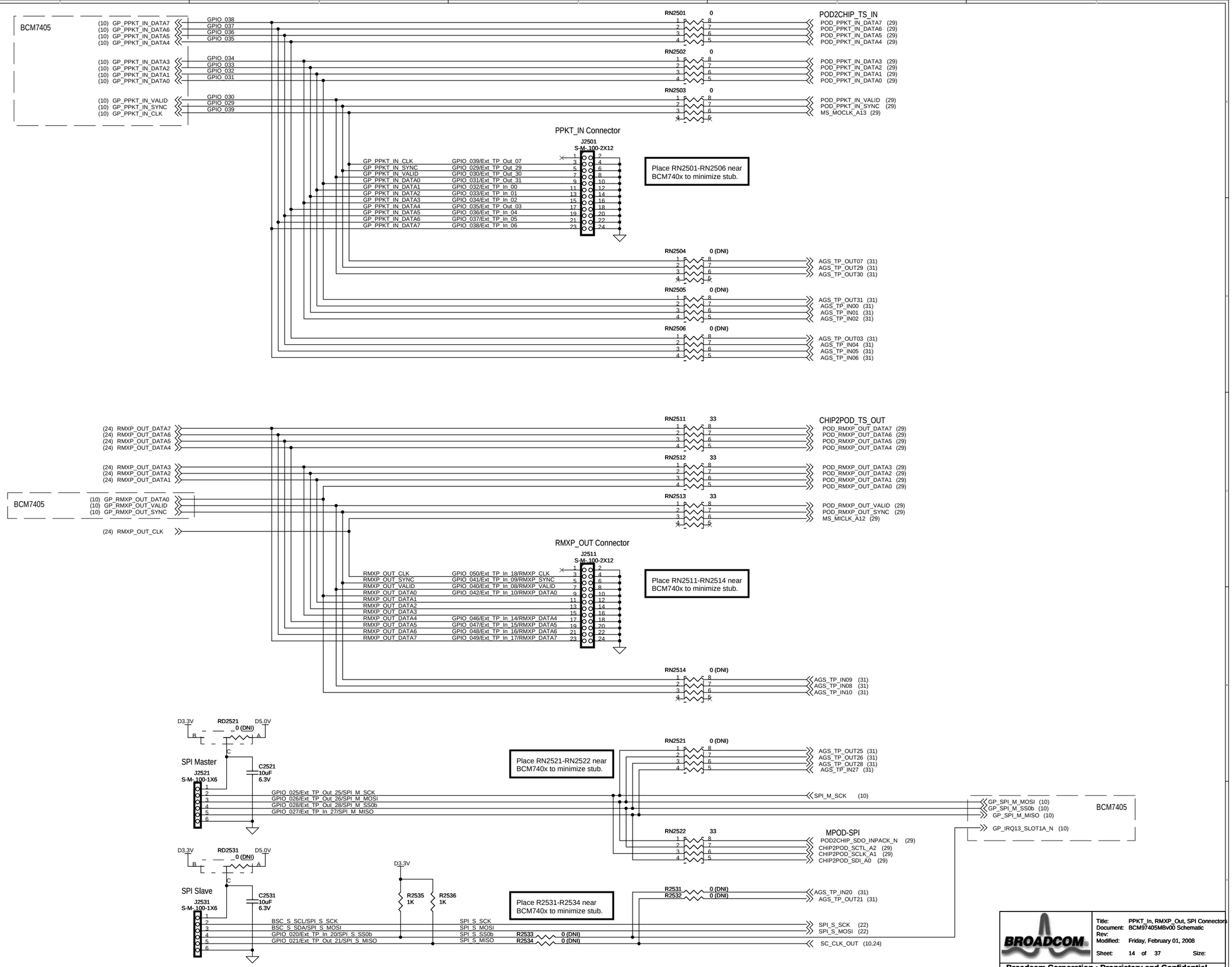
BCM7405
(10) GP_PPKT_IN_DATA7
(10) GP_PPKT_IN_DATA6
(10) GP_PPKT_IN_DATA5
(10) GP_PPKT_IN_DATA4
(10) GP_PPKT_IN_DATA3
(10) GP_PPKT_IN_DATA2
(10) GP_PPKT_IN_DATA1
(10) GP_PPKT_IN_DATA0
(10) GP_PPKT_IN_VALID
(10) GP_PPKT_IN_SYNC
(10) GP_PPKT_IN_CLK
GPIO_038
GPIO_037
GPIO_036
GPIO_035
GPIO_034
GPIO_033
GPIO_032
GPIO_031
GPIO_030
GPIO_029
GPIO_039
RN2501 0
RN2502 0
RN2503 0
POD2CHIP_TS_IN
POD_PPKT_IN_DATA7 (29)
POD_PPKT_IN_DATA6 (29)
POD_PPKT_IN_DATA5 (29)
POD_PPKT_IN_DATA4 (29)
POD_PPKT_IN_DATA3 (29)
POD_PPKT_IN_DATA2 (29)
POD_PPKT_IN_DATA1 (29)
POD_PPKT_IN_DATA0 (29)
POD_PPKT_IN_VALID (29)
POD_PPKT_IN_SYNC (29)
MS_MOCLK_A13 (29)
PPKT_IN Connector
J2501
S-M-100-2X12
GP_PPKT_IN_CLK GPIO_039/Ext_TP_Out_07
GP_PPKT_IN_SYNC GPIO_029/Ext_TP_Out_29
GP_PPKT_IN_VALID GPIO_030/Ext_TP_Out_30
GP_PPKT_IN_DATA0 GPIO_031/Ext_TP_Out_31
GP_PPKT_IN_DATA1 GPIO_032/Ext_TP_In_00
GP_PPKT_IN_DATA2 GPIO_033/Ext_TP_In_01
GP_PPKT_IN_DATA3 GPIO_034/Ext_TP_In_02
GP_PPKT_IN_DATA4 GPIO_035/Ext_TP_Out_03
GP_PPKT_IN_DATA5 GPIO_036/Ext_TP_In_04
GP_PPKT_IN_DATA6 GPIO_037/Ext_TP_In_05
GP_PPKT_IN_DATA7 GPIO_038/Ext_TP_In_06
Place RN2501-RN2506 near BCM740x to minimize stub.
RN2504 0 (DNI)
RN2505 0 (DNI)
RN2506 0 (DNI)
AGS_TP_OUT07 (31)
AGS_TP_OUT29 (31)
AGS_TP_OUT30 (31)
AGS_TP_OUT31 (31)
AGS_TP_IN00 (31)
AGS_TP_IN01 (31)
AGS_TP_IN02 (31)
AGS_TP_OUT03 (31)
AGS_TP_IN04 (31)
AGS_TP_IN05 (31)
AGS_TP_IN06 (31)
(24) RMXP_OUT_DATA7
(24) RMXP_OUT_DATA6
(24) RMXP_OUT_DATA5
(24) RMXP_OUT_DATA4
(24) RMXP_OUT_DATA3
(24) RMXP_OUT_DATA2
(24) RMXP_OUT_DATA1
BCM7405
(10) GP_RMXP_OUT_DATA0
(10) GP_RMXP_OUT_VALID
(10) GP_RMXP_OUT_SYNC
(24) RMXP_OUT_CLK
RN2511 33
RN2512 33
RN2513 33
CHIP2POD_TS_OUT
POD_RMXP_OUT_DATA7 (29)
POD_RMXP_OUT_DATA6 (29)
POD_RMXP_OUT_DATA5 (29)
POD_RMXP_OUT_DATA4 (29)
POD_RMXP_OUT_DATA3 (29)
POD_RMXP_OUT_DATA2 (29)
POD_RMXP_OUT_DATA1 (29)
POD_RMXP_OUT_DATA0 (29)
POD_RMXP_OUT_VALID (29)
POD_RMXP_OUT_SYNC (29)
MS_MICLK_A12 (29)
RMXP_OUT Connector
J2511
S-M-100-2X12
RMXP_OUT_CLK GPIO_050/Ext_TP_In_18/RMXP_CLK
RMXP_OUT_SYNC GPIO_041/Ext_TP_In_09/RMXP_SYNC
RMXP_OUT_VALID GPIO_040/Ext_TP_In_08/RMXP_VALID
RMXP_OUT_DATA0 GPIO_042/Ext_TP_In_10/RMXP_DATA0
RMXP_OUT_DATA1
RMXP_OUT_DATA2
RMXP_OUT_DATA3
RMXP_OUT_DATA4 GPIO_046/Ext_TP_In_14/RMXP_DATA4
RMXP_OUT_DATA5 GPIO_047/Ext_TP_In_15/RMXP_DATA5
RMXP_OUT_DATA6 GPIO_048/Ext_TP_In_16/RMXP_DATA6
RMXP_OUT_DATA7 GPIO_049/Ext_TP_In_17/RMXP_DATA7
Place RN2511-RN2514 near BCM740x to minimize stub.
RN2514 0 (DNI)
AGS_TP_IN09 (31)
AGS_TP_IN08 (31)
AGS_TP_IN10 (31)
D3.3V
RD2521 0 (DNI)
D5.0V
SPI Master
J2521
S-M-100-1X6
C2521 10uF 6.3V
GPIO_025/Ext_TP_Out_25/SPI_M_SCK
GPIO_026/Ext_TP_Out_26/SPI_M_MOSI
GPIO_028/Ext_TP_Out_28/SPI_M_SS0b
GPIO_027/Ext_TP_In_27/SPI_M_MISO
Place RN2521-RN2522 near BCM740x to minimize stub.
RN2521 0 (DNI)
AGS_TP_OUT25 (31)
AGS_TP_OUT26 (31)
AGS_TP_OUT28 (31)
AGS_TP_IN27 (31)
SPI_M_SCK (10)
GP_SPI_M_MOSI (10)
GP_SPI_M_SS0b (10)
GP_SPI_M_MISO (10)
BCM7405
GP_IRQ13_SLOT1A_N (10)
RN2522 33
MPOD-SPI
POD2CHIP_SDO_INPACK_N (29)
CHIP2POD_SCTL_A2 (29)
CHIP2POD_SCLK_A1 (29)
CHIP2POD_SDI_A0 (29)
RD2531 0 (DNI)
SPI Slave
J2531
S-M-100-1X6
C2531 10uF 6.3V
R2535 1K
R2536 1K
BSC_S_SCL/SPI_S_SCK
BSC_S_SDA/SPI_S_MOSI
GPIO_020/Ext_TP_In_20/SPI_S_SS0b
GPIO_021/Ext_TP_Out_21/SPI_S_MISO
SPI_S_SCK
SPI_S_MOSI
SPI_S_SS0b
SPI_S_MISO
Place R2531-R2534 near BCM740x to minimize stub.
R2531 0 (DNI)
R2532 0 (DNI)
R2533 0 (DNI)
R2534 0 (DNI)
AGS_TP_IN20 (31)
AGS_TP_OUT21 (31)
SPI_S_SCK (22)
SPI_S_MOSI (22)
SC_CLK_OUT (10,24)
BROADCOM
Title: PPKT_In, RMXP_Out, SPI Connectors
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Broadcom Corporation : Proprietary and Confidential

Active LPF/Line Driver
Fc ~ 130 kHz, Gain = 2

U100-9
BCM7405A1
bga976_35x35_1mm_dp_skt

Analog Audio
AUD0_LEFT_p — A22 — DIFF_AUD0_LEFT_P
AUD0_LEFT_n — B22 — DIFF_AUD0_LEFT_N
AUD0_RIGHT_p — B21 — DIFF_AUD0_RIGHT_P
AUD0_RIGHT_n — A21 — DIFF_AUD0_RIGHT_N

Digital Audio
AUD0_SPDIF — C21 — AUD0_SPDIF

Route as 100 Ohm differential pairs

I2S audio is found on Sheets 10, 11, 30.

R1501 34K 1% — C1502 39pF — AUD1
R1502 15K 1%
R1505 15K 1%
R1508 34K 1% — C1505 39pF
A5.0V — C1501 0.1uF — AUD1
A-5.0V — C1506 0.1uF — AUD1
U1501B NJM4580V SSOP8 (V+ pin 8, pins 5/6/7/4)
R1504 0 — C1503 10uF 6.3V
R1507 DNI — AUD1

R1509 34K 1% — C1507 39pF — AUD1
R1510 15K 1%
R1513 15K 1%
R1516 34K 1% — C1510 39pF
U1501A NJM4580V SSOP8 (V+ pin 8, pins 3/2/1/4)
R1512 0 — C1508 10uF 6.3V
R1515 DNI — AUD1

A5.0V — A-5.0V — A5.0V — A-5.0V
D1502 BAV99LT1G
D1501 BAV99LT1G
D1503 BAV99LT1G
BCM740X_CVBS (16)
J1501 RCA_TRIPLE_RWY
CVBS 0 (Yellow)
Audio0_L (White)
Audio0_R (RED)
2 Vrms

Put AUD1 GND points as close as possible to connector J1501.

Isolate Video and Audio grounds.

For power-on pop noise issue, consider using a click-pop suppressor for audio applications. (e.g. Maxim MAX9890)

MH1501
4-40X3/4in-SCREW

Strap Bit
(13) AUD0_SPDIF

D5.0V — C1521 0.1uF — R1533 470 — R1534 470
R1535 220 — C1522 0.47uF
C1524 47pF — R1536 121 1% — D1506 BAV99LT1G
C1523 0.47uF
R1537 510 — Q1501 2SA1162
J1503 SPDIF RCA/OPTICAL (2S, 2S, 3N, R, C, A, 5; VCC, VIN, GND, GND)
SPDIF RCA/Optical Audio Out

RCA Vout = 0.5 +/- 0.1V Vpp with 75 Ohm termination

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Place bias resistors R1610/R1611 and VDAC voltage regulator capacitors C1601/C1602 near BCM740x and shield them by GND.

VDAC_AVDD33

C1602 0.1uF

C1601 0.1uF

U100-4
BCM7405A1
baa976_35x35_1mm_dp_skt

Video DAC Interface

R1611 562 1%

R1610 562 1%

VDAC0_VREG D24
VDAC0_RBIAS E23
VDAC1_VREG D25
VDAC1_RBIAS C25

VDAC0_0 A24
VDAC0_1 B24
VDAC0_2 B23
VDAC1_0 B26
VDAC1_1 A25
VDAC1_2 B25

VDAC_LUMA
VDAC_CHROMA
VDAC_COMP
VDAC_BLUE
VDAC_GREEN
VDAC_RED

Place 75 ohm terminations <1" from BCM740X

R1603 75
R1604 75
R1605 75
R1606 75
R1607 75
R1608 75

R1621 0 LUMA

R1622 0 CHROMA

R1623 0 COMP

R1624 0 BLUE

R1625 0 GREEN

R1626 0 RED

3 Pole Butterworth LPF
Passband flat to 6 MHz
ZI=75 Z0 = 75

C1627 1.5pF (DNI)
L1610 1.8uH 5%
C1631 180pF 5%
C1632 180pF 5%

C1635 1.5pF (DNI)
L1611 1.8uH 5%
C1639 180pF 5%
C1640 180pF 5%

C1643 1.5pF (DNI)
L1612 1.8uH 5%
C1647 180pF 5%
C1648 180pF 5%

Place inductors so that the fields from adjacent filters DO NOT couple.

7 Pole Elliptic LPF
Passband flat to 30 MHz for 1080i/p@30 frames/sec
ZI=75, Z0=75

C1659 12pF
L1613 470nH
C1657 33pF
C1654 100pF

C1663 6.8pF
L1620 620nH
C1671 100pF

C1655 47pF
L1621 220nH
C1672 3.3pF

C1653 12pF
L1617 470nH
C1670 33pF
C1668 100pF

C1656 6.8pF
L1619 620nH
C1665 100pF

C1666 47pF
L1618 220nH
C1662 3.3pF

C1669 12pF
L1614 470nH
C1667 33pF
C1664 100pF

C1673 6.8pF
L1616 620nH
C1660 100pF

C1661 47pF
L1615 220nH
C1658 3.3pF

Place inductors & 0 ohm R's so that the fields from adjacent filters DO NOT couple.

A5.0V A-5.0V A5.0V A-5.0V

D1604 BAV99LT
D1605 BAV99LT

J1603 S-VIDEO
CHROMA
LUMA
GND
GND
SGND SGND SGND
G1 G2 G3

S-Video Out

MH1602
4-40X3/4in-SCREW

MH1601
4-40X3/4in-SCREW

D1601 BAV99LT

J1601 RCA_TRIPLE_RGB

Blue / Pb
Green / Y
Red / Pr

D1602 BAV99LT
D1603 BAV99LT

BCM740X_CVBS (15)

Title:	RGB, S-Video, CVBS
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HDMI - Layout Guidelines:
- Differential pairs should be routed on TOP or BOTTOM layers only.
- Trace impedance: 100 ohm differential impedance to the ground plane.
- 5 mils trace width with 7.5 mil air gap on P/N pair.
- Match trace length of differential pairs, 20 mils max within a pair, and 100 mils max between pairs.
- Adjacent TX/RX differential pairs should be separated by more than 50 mils to each other.

Place all ESD diodes as close as possible to J1701

U100-7
BCM7405A1
bga976_35x35_1mm_dp_skt

Digital Video

HDMI_2_P	B17	DIFF_HDMI_2P	
HDMI_2_N	C17	DIFF_HDMI_2N	
HDMI_1_P	A18	DIFF_HDMI_1P	
HDMI_1_N	B18	DIFF_HDMI_1N	
E20 HDMI_HTPLG			
HDMI_0_P	A19	DIFF_HDMI_0P	
HDMI_0_N	B19	DIFF_HDMI_0N	
HDMI_CLK_P	C20	DIFF_HDMI_CLKP	
HDMI_CLK_N	B20	DIFF_HDMI_CLKN	
HDMI_CEC	D20	HDMI_CEC_1	
HDMI_CEC_TERM	E18	HDMI_CEC_TERM	
HDMI_BIAS_RES	E19	HDMI_BIAS_RES	

D1725 8KV 1pF
D1724 8KV 1pF
D1715 8KV 1pF
D1714 8KV 1pF
D1719 8KV 1pF
D1720 8KV 1pF
D1721 8KV 1pF
D1722 8KV 1pF
D1717 8KV 1pF

J1701
HDMI-R/A-SMT

1	TMDS-D2-P
2	D2-SHIELD
3	TMDS-D2-N
4	TMDS-D1-P
5	D1-SHIELD
6	TMDS-D1-N
7	TMDS-D0-P
8	D0-SHIELD
9	TMDS-D0-N
10	TMDS-CLK-P
11	CLK-SHIELD
12	TMDS-CLK-N
13	HDMI-CEC
	NC = 14
15	TMDS-SCL
16	TMDS-SDA
17	CEC-GND
18	+5V_POWER
19	HOT-PLUG-DET
G4	GND
G3	GND
G2	GND
G1	GND

R1713 0
Q1701 NTR4501NT1G (DNI)
R1711 100K
D5.0V
HDMI_CEC

Make dual-footprint for Q1701 and R1713.

R1707 27K
C1708 56pF (DNI)

Place C1708 very close to BCM740x.

R1710 12.1K 1%

Q1701 was added for the following reasons:
- When the STB system is powered off, it must not pull down the HDMI_CEC line at the HDMI connector. (Not an issue with 65nm)
- When the STB system is powered on, the HDMI_CEC line should be terminated in to BCM740x by a 27K Ohm +/- 5% resistor.

J1706
S-M-100-1X2 (DNI)
SGPIO_03
SGPIO_02

D5.0V
R1709 2K
R1712 2K

(11) GP_BSC_M1_SCL
(11) GP_BSC_M1_SDA

C1709 18pF (DNI)
C1710 18pF (DNI)

HDMI_HOT_PLUG

D1718 8KV 1pF
D1716 8KV 1pF

Place next to J1701.

R1708 47K
D1723 BAV99LT1G
D5.0V

This ESD diode also clamps signal to +5.7v.

D5.0V
C1707 0.1uF

For improved EMI, consider using a differential line filter designed for HDMI applications. (e.g. TDK ACM2012H-900, TCM1210H-900)

DVO signals need to go to Bcm93560DVITX daughter card. Adapter card needed between here and the daughter card.

J1703
S-M-100-2X13-SHRD

DVO0_03	FP_LED_LS_1	GPIO_091/Ext_TP_Out_52	1 2	GPIO_090/Ext_TP_Out_51	FP_LED_LS_0	DVO0_02
DVO0_HSYNC	FP_LED_LS_3	GPIO_093/Ext_TP_Out_54	3 4	GPIO_092/Ext_TP_Out_53	FP_LED_LS_2	DVO0_VSYNC
DVO0_DE	FP_LED_KD_0	GPIO_086/Ext_TP_Out_47	5 6	GPIO_094/Ext_TP_Out_55	FP_LED_LS_4	DVO0_04
DVO0_00	FP_LED_KD_2	GPIO_088/Ext_TP_Out_49	7 8	GPIO_087/Ext_TP_Out_48	FP_LED_KD_1	DVO0_CLK_N
DVO0_05	FP_LED_LD_0	GPIO_095/Ext_TP_Out_56	9 10	GPIO_089/Ext_TP_Out_50	FP_LED_KD_3	DVO0_01
DVO0_07	FP_LED_LD_2	GPIO_097/Ext_TP_Out_58	11 12	GPIO_096/Ext_TP_Out_57	FP_LED_LD_1	DVO0_06
DVO0_09	FP_LED_LD_4	GPIO_099/Ext_TP_Out_60	13 14	GPIO_098/Ext_TP_Out_43	FP_LED_LD_3	DVO0_08
DVO0_11	FP_LED_LD_6	GPIO_101/Ext_TP_Out_62	15 16	GPIO_100/Ext_TP_Out_61	FP_LED_LD_5	DVO0_10
			17 18	GPIO_102/Ext_TP_Out_63	FP_LED_LD_7	DVO0_CLK_P
		BCM740X_IRIN	19 20			
(23) BCM740X_IRIN			21 22			
			23 24			
			25 26			

D5.0V
C1705 4.7uF
R1706 4.7K
D3.3V
C1704 4.7uF

(4,5,18,20,21,24,25,27,28,29,30) BCM740X_RST_OUT_N

(21) FP_4SEC_RST_N

SW1701
PB-SPST-MOM
"4-SEC-RST"

Front Panel / DVO Interface

Front Panel should be designed such that its operation will not affect strapping.

Use Bcm97455v10-xx Front Panel

FP_LED_KD_0 (11)
FP_LED_KD_1 (11)
FP_LED_KD_2 (11)
FP_LED_KD_3 (11)

FP_LED_LD_0 (11)
FP_LED_LD_1 (11)
FP_LED_LD_2 (11)
FP_LED_LD_3 (11)
FP_LED_LD_4 (11)
FP_LED_LD_5 (11)
FP_LED_LD_6 (11)
FP_LED_LD_7 (11)

FP_LED_LS_0 (11)
FP_LED_LS_1 (11)
FP_LED_LS_2 (11)
FP_LED_LS_3 (11)
FP_LED_LS_4 (11)

BROADCOM

Title: HDMI A/V, Front Panel
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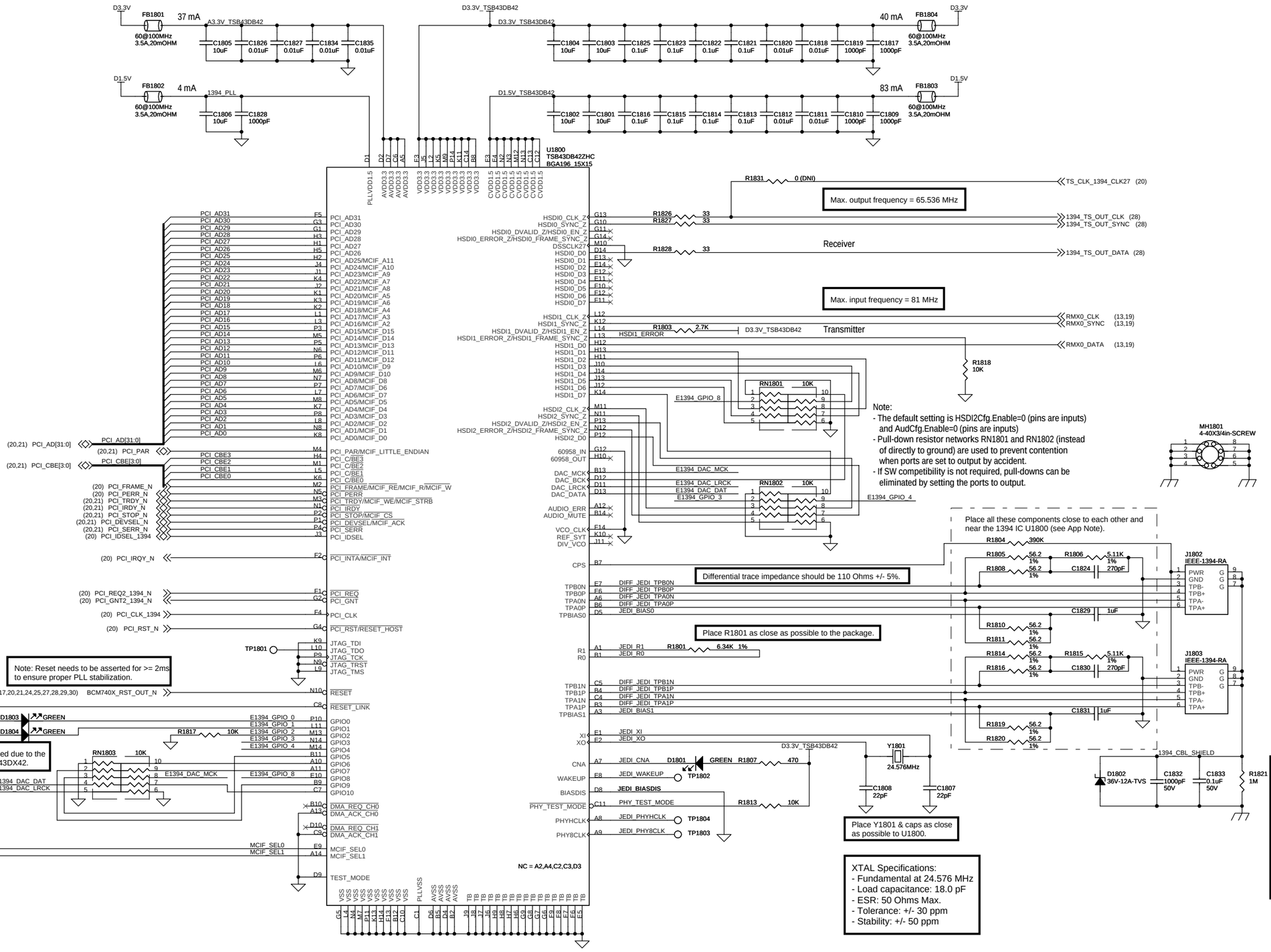

Title:	IEEE 1394 Link & Phy
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Place R's and RN's near BCM740x to minimize stub.

Place test headers J1900-J1905 near BCM740x to minimize stub.

RN1907 0 (DNI)
(31) AGS_TP_IN29
(31) AGS_TP_OUT20
(31) AGS_TP_IN28
(31) AGS_TP_IN19

RN1906 0 (DNI)
(31) AGS_TP_IN31
(31) AGS_TP_OUT22
(31) AGS_TP_IN30
(31) AGS_TP_IN21

J1900 S-M-.100-2X3
PKT_VALID0 GPIO_057 GPIO_063/Ext_TP_In_28 GP_PKT_CLK0
GP_PKT_ERROR0 GPIO_051/Ext_TP_In_19 GPIO_075 GP_PKT_SYNC0
GPIO_069/Ext_TP_Out_34 GP_PKT_DATA0

J1901 S-M-.100-2X3
PKT_VALID1 GPIO_058 GPIO_064/Ext_TP_In_29 GP_PKT_CLK1
GP_PKT_ERROR1 GPIO_052/Ext_TP_Out_20 GPIO_076 GP_PKT_SYNC1
GPIO_070/Ext_TP_Out_35 GP_PKT_DATA1

J1902 S-M-.100-2X3
PKT_VALID2 GPIO_059 GPIO_065/Ext_TP_In_30 GP_PKT_CLK2
GP_PKT_ERROR2 GPIO_053/Ext_TP_In_21 GPIO_077 GP_PKT_SYNC2
GPIO_071/Ext_TP_Out_36 GP_PKT_DATA2

J1903 S-M-.100-2X3
PKT_VALID3 GPIO_060 GPIO_066/Ext_TP_In_31 GP_PKT_CLK3
GP_PKT_ERROR3 GPIO_054/Ext_TP_Out_22 GPIO_078/Ext_TP_Out_39 GP_PKT_SYNC3
GPIO_072/Ext_TP_Out_37 GP_PKT_DATA3

J1904 S-M-.100-2X3
PKT_VALID4 GPIO_061 GPIO_067/Ext_TP_Out_32 GP_PKT_CLK4
PKT_ERROR4 GPIO_055 GPIO_079/Ext_TP_Out_40 GP_PKT_SYNC4
GPIO_073/Ext_TP_Out_38 GP_PKT_DATA4

J1905 S-M-.100-2X3
PKT_VALID5 GPIO_062 GPIO_068/Ext_TP_Out_33 GP_PKT_CLK5
PKT_ERROR5 GPIO_056 GPIO_080/Ext_TP_Out_41 GP_PKT_SYNC5
GPIO_074 GP_PKT_DATA5

RN1900 0
(4) BCM3510_PKT_CLK0
(4) BCM3510_PKT_SYNC0
(4) BCM3510_PKT_DATA0
(4) BCM3510_PKT_VALID0
R1900 0
(4) BCM3510_PKT_ERROR0

RN1901 0
(27) SLOT0_PKT_CLK1
(27) SLOT0_PKT_SYNC1
(27) SLOT0_PKT_DATA1
(27) SLOT0_PKT_VALID1
R1901 0
(27) SLOT0_PKT_ERROR1

RN1902 0
(27) SLOT0_PKT_CLK2
(27) SLOT0_PKT_SYNC2
(27) SLOT0_PKT_DATA2
(27) SLOT0_PKT_VALID2
R1902 0
(27) SLOT0_PKT_ERROR2

RN1903 0
(27) SLOT1_PKT_CLK3
(27) SLOT1_PKT_SYNC3
(27) SLOT1_PKT_DATA3
(27) SLOT1_PKT_VALID3
R1903 0
(27) SLOT1_PKT_ERROR3

RN1904 0
(27) SLOT1_PKT_CLK4
(27) SLOT1_PKT_SYNC4
(27) SLOT1_PKT_DATA4
(27) SLOT1_PKT_VALID4
R1904 0
(27) SLOT1_PKT_ERROR4

RN1905 0
(28) ALT_PKT_CLK5
(28) ALT_PKT_SYNC5
(28) ALT_PKT_DATA5
(28) ALT_PKT_VALID5
R1905 0
(28) ALT_PKT_ERROR5

R1906 0 (DNI)
R1907 0 (DNI)
(10,23) UART_RXD_2
(10,23) UART_TXD_2

BCM7405 Transport Inputs
GP_PKT_CLK0 (11)
GP_PKT_SYNC0 (11)
GP_PKT_DATA0 (11)
PKT_VALID0 (30)
GP_PKT_ERROR0 (10)
GP_PKT_CLK1 (11)
GP_PKT_SYNC1 (11)
GP_PKT_DATA1 (11)
PKT_VALID1 (30)
GP_PKT_ERROR1 (10)
GP_PKT_CLK2 (11)
GP_PKT_SYNC2 (11)
GP_PKT_DATA2 (11)
PKT_VALID2 (30)
GP_PKT_ERROR2 (10,29)
GP_PKT_CLK3 (11)
GP_PKT_SYNC3 (11)
GP_PKT_DATA3 (11)
PKT_VALID3 (30)
GP_PKT_ERROR3 (10,29)
GP_PKT_CLK4 (11)
GP_PKT_SYNC4 (11)
GP_PKT_DATA4 (11)
PKT_VALID4 (30)
PKT_ERROR4 (30)
GP_PKT_CLK5 (11,30)
GP_PKT_SYNC5 (11,30)
GP_PKT_DATA5 (11,30)
PKT_VALID5 (30)
PKT_ERROR5 (30)

U100-6
BCM7405A1
bga976_35x35_1mm_dp_skt
Transport Outputs
RMX_CLK0 AP32
RMX_SYNC0 AM32
RMX_DATA0 AN32
RMX_CLK1 AK31
RMX_SYNC1 AK30
RMX_DATA1 AL31

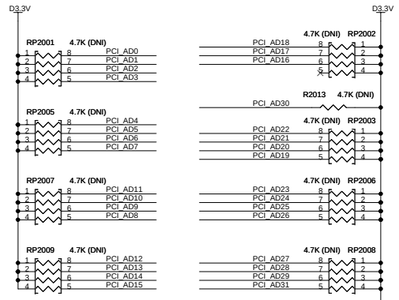
RN2202 33
RN2204 33

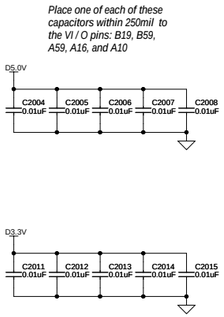
J2209 S-M-.100-1X4
J2202 S-M-.100-1X4
RMX1_SYNC
RMX1_DATA
RMX1_CLK

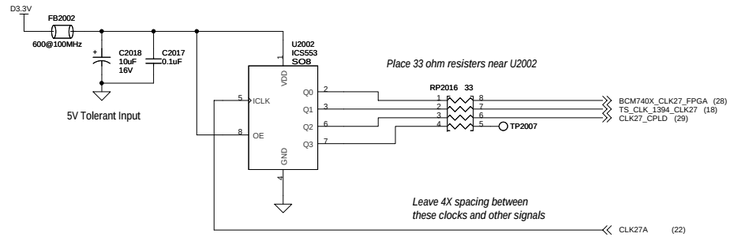
RMX0_SYNC (13,18)
RMX0_DATA (13,18)
RMX0_CLK (13,18)
Strap Bit
Strap Bit
Strap Bit
RMX1_SYNC (13)
RMX1_DATA (13)
RMX1_CLK (13)
Strap Bit
Strap Bit
Strap Bit

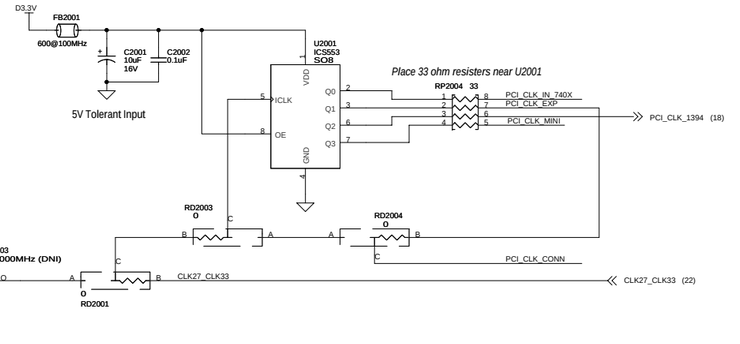
BROADCOM

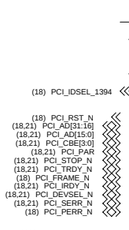
Title: PKT, RMX
Document: BCM97405MBv00 Schematic
Rev:
Modified: Friday, February 01, 2008
Sheet: 19 of 37 Size:

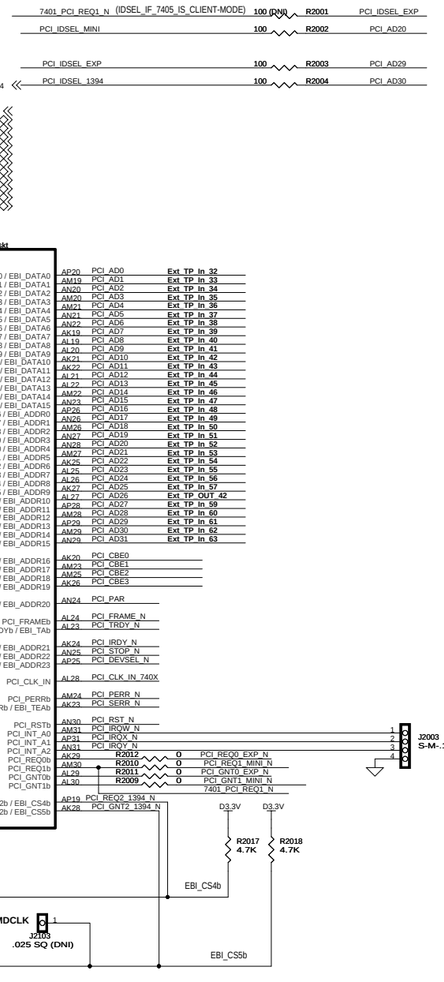




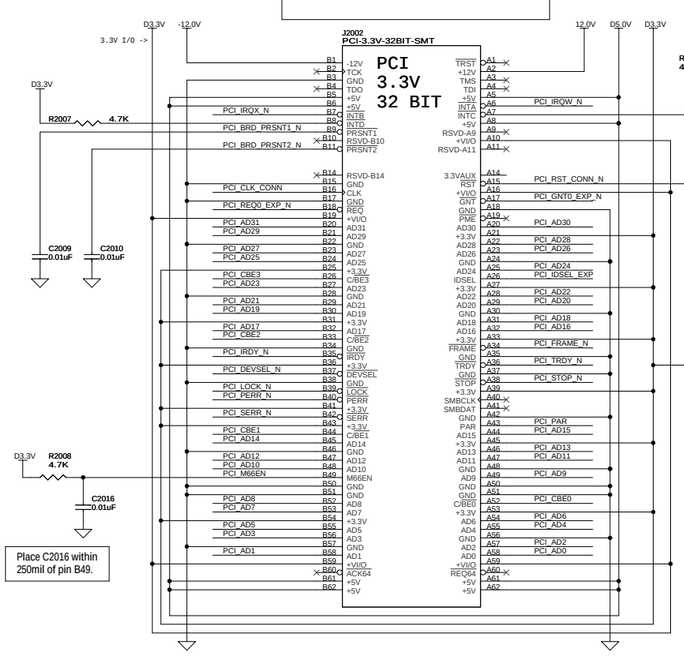


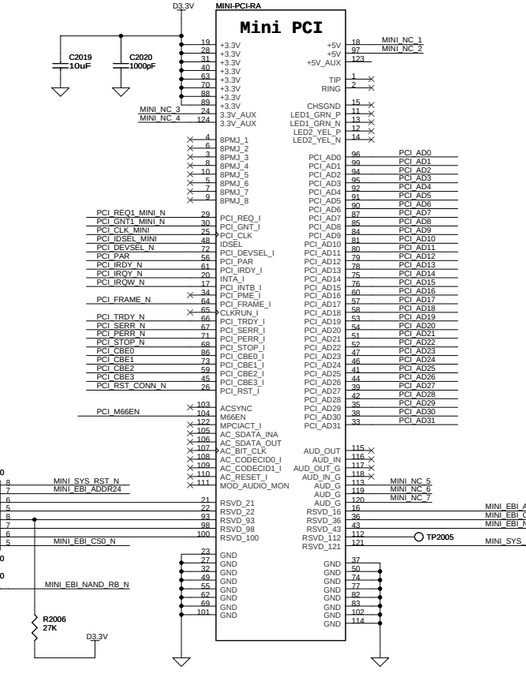






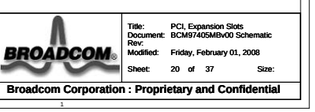
Clearly silkscreen the A1 / B1 locations on the board.

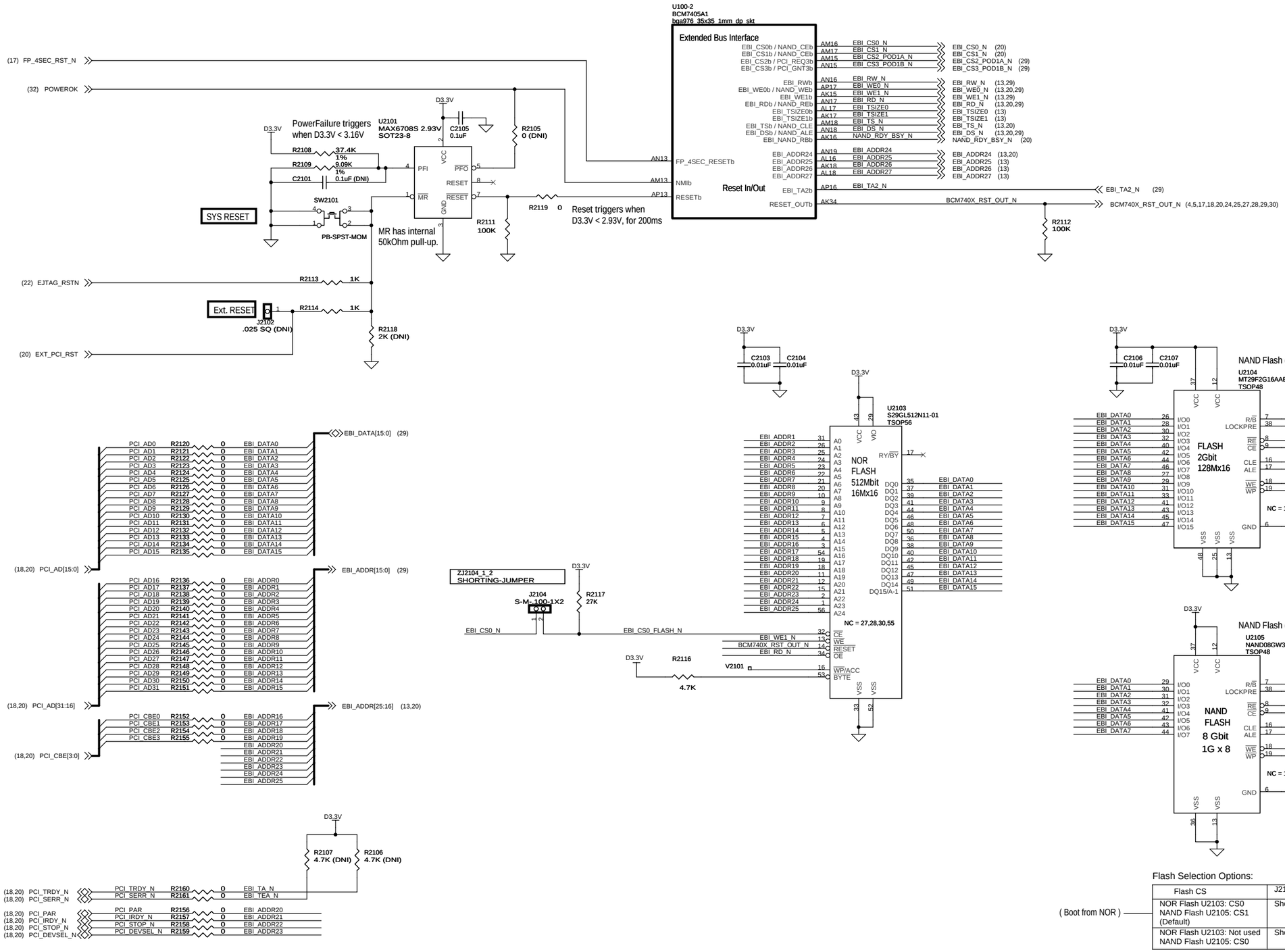




Use PCI_REQ2 / PCI_GNT2 for 1394 to be software compatible with Bcm97038.

(18) PCI_IRQY_N





Flash Selection Options:

(Boot from NOR)

Flash CS	J2101	J2104
NOR Flash U2103: CS0 NAND Flash U2105: CS1 (Default)	Short 1-2	Short 1-2
NOR Flash U2103: Not used NAND Flash U2105: CS0	Short 2-3	DNI

BROADCOM

Title:	EBI, Flash, Reset
Document:	BCM97405MBv00 Schematic
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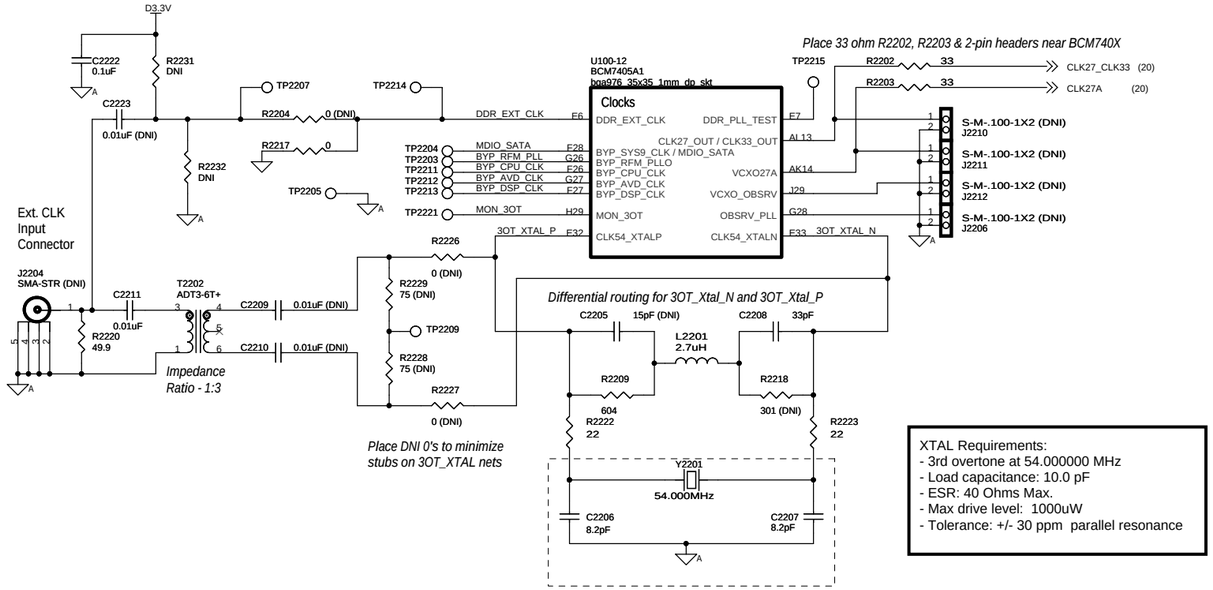
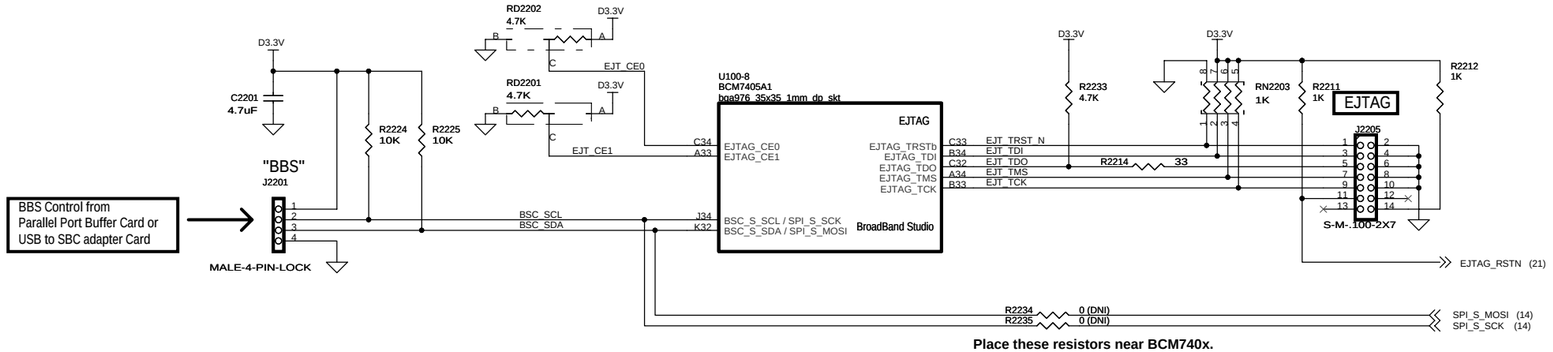


Function	EJTAG_CEO	EJTAG_CE1
Normal EJTAG Operation	1	0
Internal test only	X	1
JTAG boundary scan	0	0



Place these resistors near BCM740x.

Title: CLKs, JTAG, BBS-BSC
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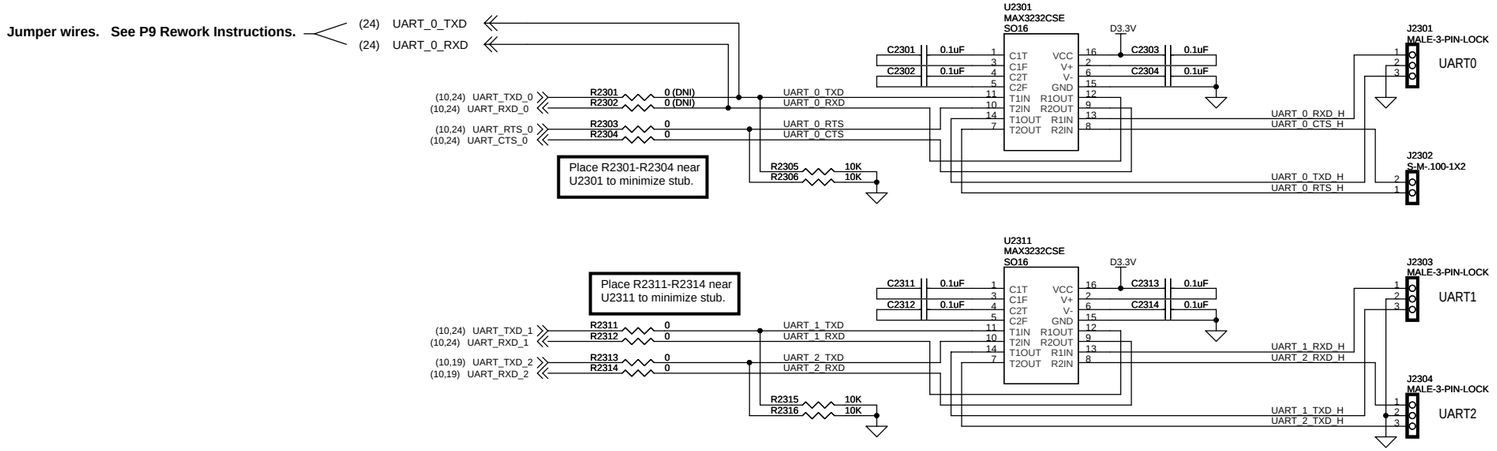
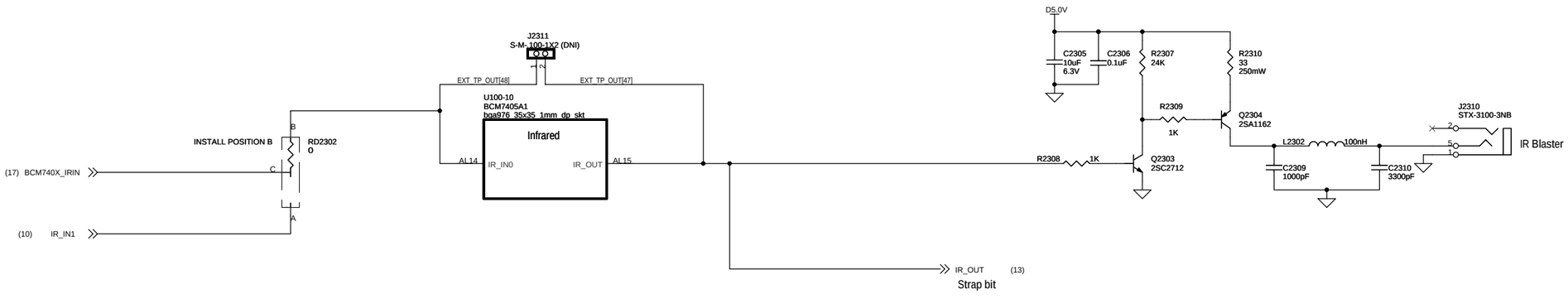
The BCM97405 reference board only uses the 2-wire UART ports (no flow control). A 4-wire option (with flow control) is available on UART0 with J2302.

Jumper wires. See P9 Rework Instructions.



The UARTs connect to two sets of GPIO pins on the Bcm7405. One set has MII as another function. If MII is used, then use other set, which has Smart Card 0/1, PKT_ERROR0/1 as another function.



Title:	UART, IR-Tx, IR-Rx
Document:	BCM97405MBv00 Schematic
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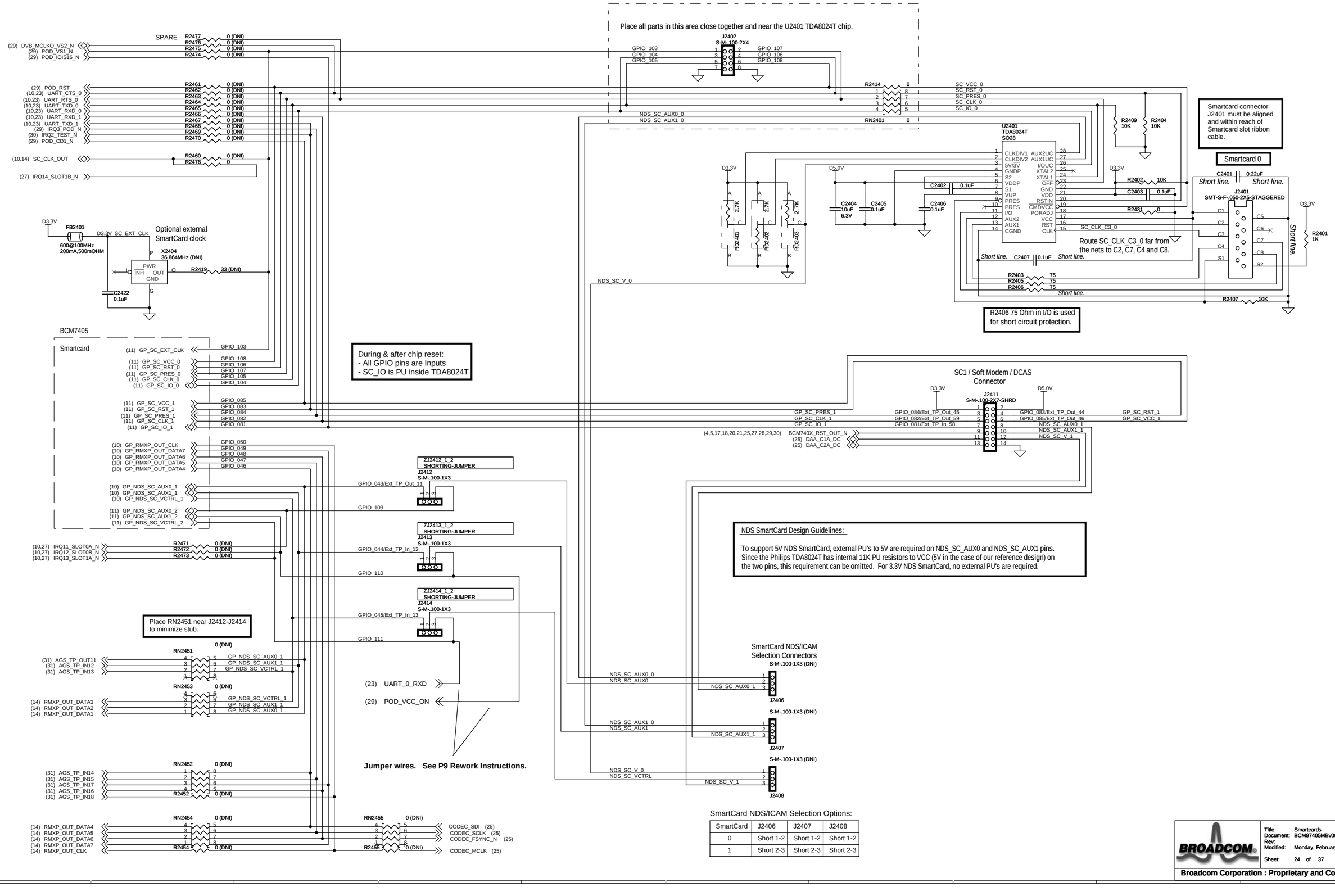

SmartCard NDS/ICAM Selection Options:

SmartCard	J2406	J2407	J2408
0	Short 1-2	Short 1-2	Short 1-2
1	Short 2-3	Short 2-3	Short 2-3

Title:	Smartcards
Document:	BCM97405MBv00 Schematic
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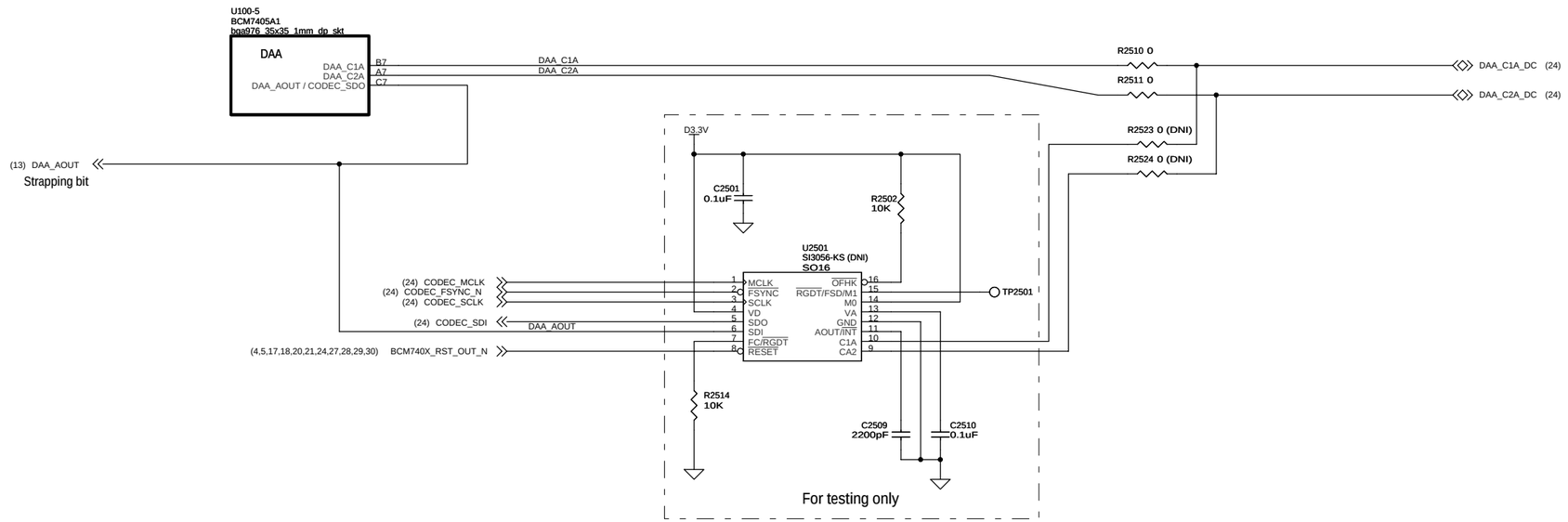

Title:	Soft Modem Interface
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(31) AGS_TP_OUT00 — R2625 0 (DNI)
(31) AGS_TP_OUT01 — R2626 0 (DNI)

BCM7405
(10) GP_ENET_ACTIVITY — GPIO_000 — R2623 0 — ACTLEDb
(10) GP_ENET_LINK — GPIO_001 — R2624 0 — LNKLEDb

GP_ENET_ACTIVITY — GPIO_000/Ext_TP_Out_00
GP_ENET_LINK — GPIO_001/Ext_TP_Out_01
J2602 S-M-.100-1X2

MH2601 4-40X3/4in-SCREW

Ethernet PHY RX and TX terminated on the die. No need for terminations on the board. Leave pads for board terminations until testing of on-die terminations is finalized.

R2605 DNI, R2606 DNI, C2603 0.1uF, R2607 DNI, R2608 DNI, C2604 0.1uF

ENet - Layout Guidelines:
- 5 mils trace width with 7 mils air gap on P/N pair.
- Trace impedance: 100 Ohm differential impedance to the ground plane.
- Adjacent TX/RX differential pairs should be separated by more than 15 mils to each other.
- TX/RX differential pairs should be routed on TOP or BOTTOM layers only.
- Match trace length of differential pairs, 100 mils max within a pair, and 500 mils max between pairs.

U100-15
BCM7405A1
bga976_35x35_1mm_dp_skt

Ethernet
R2609 1% 1.24K — EPHY_RDAC — E14 EPHY_RDAC
TP2602 — EPHY_VREF — E13 EPHY_VREF
EPHY_RDP C14 — DIFF_ENET_RX_P
EPHY_RDN B14 — DIFF_ENET_RX_N
EPHY_TDP B15 — DIFF_ENET_TX_P
EPHY_TDN A15 — DIFF_ENET_TX_N

USB
TP2605 — C2609 100pF — R2617 4.02K 1% — USB_RREF D12
J2606 S-M-.100-1X2 (DNI) — USB_MONPLL E13, USB_MONCDR E12
J2607 S-M-.100-1X2 (DNI)
USB0_DP A13 — DIFF_USB0D_P
USB0_DN B13 — DIFF_USB0D_N
USB0_PWRON A9 — USB0_PWRON_N
USB0_PWRFLT C10 — USB0_PWRFLT_N
USB1_DP A12 — DIFF_USB1D_P
USB1_DN B12 — DIFF_USB1D_N
USB1_PWRON B9 — USB1_PWRON_N
USB1_PWRFLT A10 — USB1_PWRFLT_N
USB2_DP B11 — DIFF_USB2D_P
USB2_DN B10 — DIFF_USB2D_N
USB2_PWRON C8 — USB2_PWRON_N
USB2_PWRFLT B8 — USB2_PWRFLT_N

SATA
3 Gbps
D3.3V — FB2651 600@100MHz 200mA,500mOHM — D3.3V_SATA_EXT_CLK
X2651 7EA0000023 100.00MHz (DNI) — VCC, OUT, OUT, GND
C2651 0.1uF
C2652 0.01uF (DNI) — SATA_REFCLK_P — K31 SATA_REFCLKP
R2651 100 (DNI)
C2653 0.01uF (DNI) — SATA_REFCLK_N — K30 SATA_REFCLKN
R2652 150 (DNI), R2653 150 (DNI)
SATA_PLLTESTP M28, SATA_PLLTESTN L29
TP2607, TP2606

SATA_TXDP1 G33 — DIFF_SATA_TX1_P — C2610 0.01uF
SATA_TXDN1 G34 — DIFF_SATA_TX1_N — C2612 0.01uF
SATA_RXDP1 F33 — DIFF_SATA_RX1_P — C2613 0.01uF
SATA_RXDN1 F34 — DIFF_SATA_RX1_N — C2614 0.01uF
SATA_TXDP2 J33 — DIFF_SATA_TX2_P — C2615 0.01uF
SATA_TXDN2 J32 — DIFF_SATA_TX2_N — C2616 0.01uF
SATA_RXDP2 H32 — DIFF_SATA_RX2_P — C2617 0.01uF
SATA_RXDN2 H33 — DIFF_SATA_RX2_N — C2619 0.01uF

Oscillator Specifications:
- 3rd overtone at 100.00 MHz
- Supply Voltage: 3.3V
- Output Type: LVPECL or LVDS
- Tolerance: +/- 50 ppm
- Stability: +/- 50 ppm
- Phase Jitter: < 1ps

If SATA external oscillator not used, leave SATA_REFCLKP/N inputs floating.

Recommend replacing backup oscillator with inexpensive 25 or 30 MHz crystal. No oscillator or crystal is normally needed. However, customer boards may find it is needed to meet SATA specs.

USB & SATA - Layout Guidelines:
- Dp and Dn differential pairs should be routed on TOP or BOTTOM layer only.
- Match trace length of Dp and Dn differential pairs, 20 mils max within a pair, and 100 mils max between pairs.
- The length for the differential pairs should be less than 5 inches.
- Do not place more than 2 vias per trace, prefer zero.
- Never split the ground plane under differential pairs when routing.
- Route differential pairs above the GND plane.
- Differential impedance is 90 Ohms (5.5 mils trace width with 5.5 mils air gap) for USB and 100 Ohms for SATA (5 mils trace width with 7 mils air gap).
- Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 5 mils trace, leave >15 mils between adjacent differential pairs)
- Stitch GND vias around each differential pair, but NOT between a given pair.

Add 1k ohm differential termination between RXDP and RXDN, also TXDP and TXDN, on these SATA lines next to 7405. To be used as tweak to fine-tune the on-die SATA termination.

J2603 SERIAL ATA — HT+, HT-, HR+, HR-, GND
J2605 SERIAL ATA — HT+, HT-, HR+, HR-, GND

For better performance, use SMT connector 536420-00.

For improved EMI, consider using a differential line filter designed for SATA applications. (e.g. TDK ACM2012H-900)

Advise ESD protection on lines going to eSATA connector.

Strap Bits — (13) USB0_PWRON_N, (13) USB1_PWRON_N

A2.5V_BCM740X — FB2601 60@100MHz 3.5A,20mOHM — A2.5V_EPHY_TERM
C2601 22uF, C2602 1000pF, R2603 0, R2604 0, C2605 1000pF, C2606 1000pF
TP2601 WHITE

Connector has built-in Ethernet transformer. Route this area void of all PWR/GND planes and high speed nets, except for the chassis ground. Also keep traces short and route as matched length differential pairs.

J2609 RJ45-10/100BASE-TX
TX_+, TX_CT, TX_-, RX_+, RX_CT, RX_-, LED1_CAT, LED1_AN, LED2_CAT, LED2_AN, VBUS1, DM1+, DM1-, GND1, VBUS2, DM2+, DM2-, GND2, SHLD

Ethernet DTE Device

Activity LED: Yellow

Link LED: Green

Bottom: USB2 Port 1, 500 mA

Middle: USB2 Port 0, 500 mA

D3.3V — R2614 62, R2615 62

Make the width of power traces to U2601 >= 12 mils.

D5.0V — C2625 100uF, C2626 0.1uF
U2601 MAX1823EUB+ uMAX10 — IN, INA, INB, OUTA, OUTB, ONA, ONB, FAULTA, FAULTB, GND
D3.3V — R2618 2.7K, R2619 2.7K

FB2621 60@100MHz 3.5A,20mOHM — USB0_VBUS — C2621 100uF, C2623 0.01uF
FB2622 60@100MHz 3.5A,20mOHM — USB0_GND
FB2623 60@100MHz 3.5A,20mOHM — USB1_VBUS — C2620 100uF, C2622 0.01uF
FB2624 60@100MHz 3.5A,20mOHM — USB1_GND

For improved EMI, consider using a differential line filter designed for USB applications. (e.g. TDK ACM2012-900)

J2604 S-M-.100-1X5

USB2.0 Port 2, 500 mA

WARNING - MAKE SURE J2604 PINOUT MATCHES CABLE USED FOR USB CONNECTOR.

Make the width of power traces to U2602 >= 12 mil.

D5.0V — C2628 100uF, C2631 0.1uF
U2602 MAX1823EUB+ uMAX10 — IN, INA, INB, OUTA, OUTB, ONA, ONB, FAULTA, FAULTB, GND
MAX1823_NC
D3.3V — R2632 2.7K

USBx_VBUS, USBx_GND lines have high current up to 500mA starting from MAX1823 switch. The trace width should be greater than 12 mils.

FB2625 60@100MHz 3.5A,20mOHM — USB2_VBUS — C2627 100uF, C2630 0.01uF
FB2626 60@100MHz 3.5A,20mOHM — USB2_GND

Cable this to a bulkhead USB connector. Can be Type A or B, depending upon strap-bit setting for USB Mode. (See Sheet 13)

Cable used because PCB too crowded to route USB traces to front panel.

Cable this to bulkhead eSATA connector.

BROADCOM

Title:	Ethernet, USB, SATA
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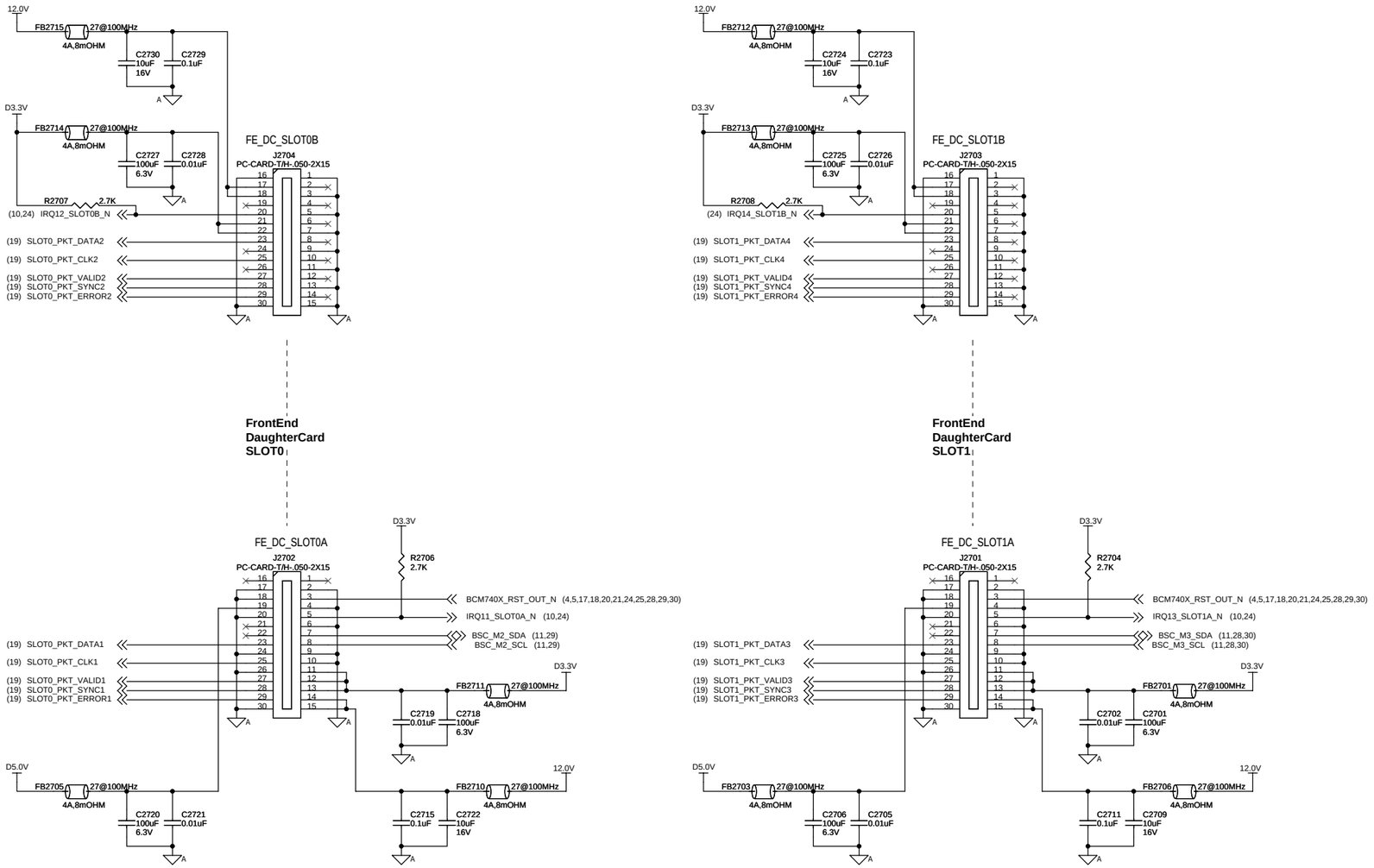

Title:	FrontEnd DaughterCard Slots
Document:	BCM97405MBv00 Schematic
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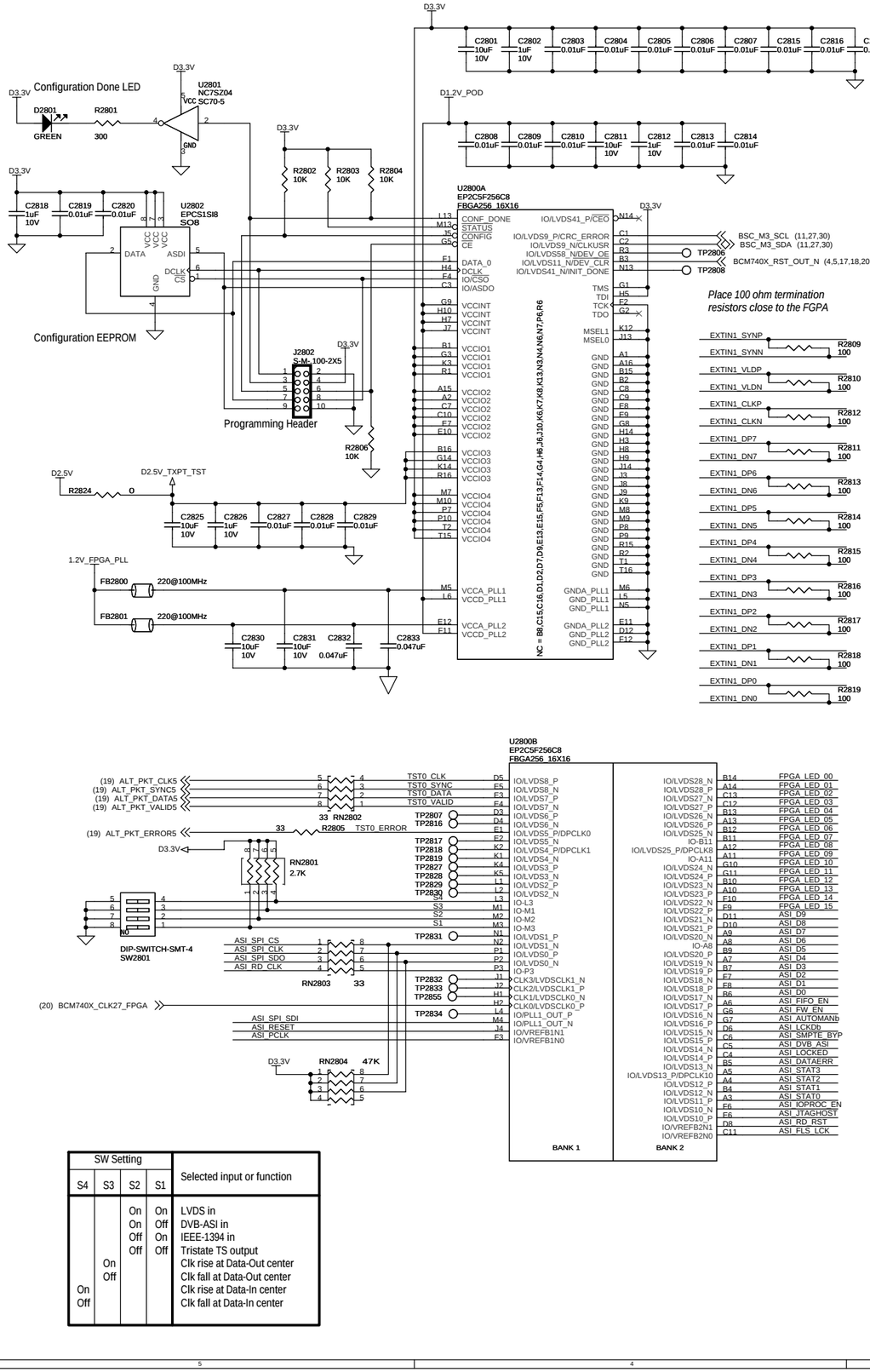

SW Setting				Selected input or function
S4	S3	S2	S1	
		On	On	LVDS in
		On	Off	DVB-ASI in
		Off	On	IEEE-1394 in
		Off	Off	Tristate TS output
	On			Clk rise at Data-Out center
	Off			Clk fall at Data-Out center
On				Clk rise at Data-In center
Off				Clk fall at Data-In center

BROADCOM

Title: Transport Test FPGA
Document: BCM97405MBv00 Schematic
Rev:
Modified: Monday, February 04, 2008
Sheet: 28 of 37 Size:Custom

This default configuration of this circuit supports MPOD and SPOD.
For Glueless MPOD-only interface, Install the 0 ohms below (in this box) which will:

1. Tri-states all outputs of the CPLD and 74LV125 (CPLD and 74LV125 can be removed optionally).
2. Connects POD signals without any glue logic/buffer.

74XX_SDO dirves POD_SDI

RN2911
0 (DNI)
GLUELESS_MPOD_ONLY_N
OB_DRX_A9
OB_CRX_A8
TX_CLK_A4

Layout must keep the stubs short due to these 0-ohms and signal jamming to/from 74LVC125.

This design supports SCARD, MCARD, and DVB-CI. To understand details of how to interface the Bcm7405 to each of these standards, please see the App Note "740X-AN400-Dx" "Cable Card Interface for the BCM7400, BCM7401, BCM7403, and BCM7405".

D2901 GREEN
R2903 300

U2901
LC4128V-75TN144C
TQFP-144
NC = 17,20,38,45,72,89,92,110,117,144

C2912 10uF 10V
C2913 1uF 10V
C2914 0.01uF
C2915 0.01uF
C2916 0.01uF
C2906 0.01uF
C2909 0.01uF
C2918 0.01uF

(21) EBI_DATA[15:0]
(13,20,21) EBI_ADDR[25:16]
(21) EBI_ADDR[15:0]

R2907 4.7K
(21) EBI_TA2_N
R2905 4.7K
R2910 27K (DNI)
(21) EBI_CS2_POD1A_N
(21) EBI_CS3_POD1B_N
R2925 0
R2926 0

(13,21) EBI_RW_N
(13,20,21) EBI_WE0_N
(13,21) EBI_WE1_N
(13,20,21) EBI_RD_N
(13,20,21) EBI_DS_N
3255_POD_OOB_DT
3255_POD_OOB_CK

(20) CLK27_CPLD
(4,5,17,18,20,21,24,25,27,28,30) BCM740X_RST_OUT_N
LED_Test
R2911 4.7K
R2924 10K
GLUELESS_MPOD_ONLY_N

Keep RMXP and PPKT stubs short

R2934 10K

Add 33 ohm termination on GP_PKT_ERROR3 at Bcm7405.

(10,19) GP_PKT_ERROR3
(14) POD_RMXP_OUT_VALID
(14) POD_RMXP_OUT_SYNC
(14) POD_RMXP_OUT_DATA0
(14) POD_RMXP_OUT_DATA1
(14) POD_RMXP_OUT_DATA2
(14) POD_RMXP_OUT_DATA3
(14) POD_RMXP_OUT_DATA4
(14) POD_RMXP_OUT_DATA5
(14) POD_RMXP_OUT_DATA6
(14) POD_RMXP_OUT_DATA7

(14) POD_PPKT_IN_VALID
(14) POD_PPKT_IN_SYNC
(14) POD_PPKT_IN_DATA0
(14) POD_PPKT_IN_DATA1
(14) POD_PPKT_IN_DATA2
(14) POD_PPKT_IN_DATA3
(14) POD_PPKT_IN_DATA4
(14) POD_PPKT_IN_DATA5
(14) POD_PPKT_IN_DATA6
(14) POD_PPKT_IN_DATA7

R2908 33

J2901
PCMCIA-SOCKET-3V

PC_CE1_N
PC_CE2_N
PC_RD_N
PC_WE0_N
PC_DS_N
PC_WE1_N
(14) POD2CHIP_SDO_INPACK_N
(24) IRQ3_POD_N
R2915 100K

3V

PC_D0
PC_D1
PC_D2
PC_D3
PC_D4
PC_D5
PC_D6
PC_D7
PC_A3
TX_CLK_A4
TX_I_A5
TX_EN_A6
TX_Q_A7
OB_CRX_A8
OB_DRX_A9
PC_A10
PC_A11

RN2902 10K
RN2906 10K
CHIP2POD_SDI_A0 (14)
CHIP2POD_SCLK_A1 (14)
CHIP2POD_SCTL_A2 (14)

R2914 33
MS_MICLK_A12 (14)
MS_MOCLK_A13 (14)
IRQ3_POD_N
R2916 33
DVB_MCLKO_VS2_N
PC_WAIT_N
POD_CD1_N (24)
POD_CD2_N (30)
POD_VS1_N (24)
POD_IOIS16_N (24)
POD_RST (24)

(24) DVB_MCLKO_VS2_N

RD2901 0
J2906 S-M-.100-1X2
Insert jumper plug to force Vcc On for MII daughter board testing
U2903 LTC1477CS8 SO8
(11) GP_POD_VCC_ON
POD_VCC_ON
R2909 1K (DNI)
C2921 1uF 16V
C2922 0.1uF

C2919 0.1uF
U2904 LTC1471 SO-16
C2920 0.1uF
R2927 2.2K
VPP1_MPOD_LOGIC
C2924 1uF 16V
C2923 1uF 16V

For MPOD only interface, LTC1471 can be changed to LTC1470.

EN0	EN1	OUT
0	0	HI-Z
0	1	3.3V
1	0	5V
1	1	HI-Z

(30) IRQ10_3510_N

Jumper wires. See P9 Rework Instructions.
(23) UART_0_TXD
(24) POD_VCC_ON

TDO
TDI
TMS
TCK
Cut pin 5
J2902 S-M-.100-1X8
R2901 1K
R2902 1K
R2906 1K
R2904 1K

R2935 10K
R2930 10K
R2931 10K
OB_DRX_A9
OB_CRX_A8
SS_EN_N
MS_EN_N
DVB_EN_N
POD_MCLKO_A14
PC_DVB_A13
PC_DVB_A12
PC_DVB_A7
PC_DVB_A6
PC_DVB_A5
PC_DVB_A4
POD2CHIP_SDO_INPACK_N
Do I need this?
PC_A3
PC_WAIT_N
POD_VPP1_EN0
POD_VPP1_EN1
POD_VPP2_EN0
PC_D0
PC_D1
PC_D2
POD_VPP2_EN1
3255_POD_US_CLK

R2921 2.7K
R2922 2.7K
BSC_M2_SCL (11,27)
BSC_M2_SDA (11,27)

Keep the jamming signals like this one really short

C2903 0.01uF
U2902A 74LVC125A SO14
GP_PKT_ERROR2 (10,19)

U2902B 74LVC125A SO14

R2929 10K
R2928 10K
U2902D 74LVC125A SO14

R2933 10K
R2932 10K
U2902C 74LVC125A SO14

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Teletext signals are on GPIO57/58

J3011
S-M-100-2X5

GP_VI_656_D0	GPIO_055/Ext_TP_In_23	1	2	GPIO_059/Ext_TP_Core_Sel_2
GP_VI_656_D1	GPIO_056/Ext_TP_Out_24	3	4	GPIO_060/Ext_TP_In_25
GP_VI_656_D2	GPIO_057/Ext_TP_Core_Sel_0	5	6	GPIO_061/Ext_TP_In_26
GP_VI_656_D3	GPIO_058/Ext_TP_Core_Sel_1	7	8	GPIO_062/Ext_TP_Out_27
		9	10	GPIO_024/Ext_TP_In_24

(31) AGS_TP_IN24 — R3011 0 (DNI)

(31) AGS_TP_IN23 — RN3011 0 (DNI)
(31) AGS_TP_OUT24
(31) AGS_TP_IN25
(31) AGS_TP_IN26
(31) AGS_TP_OUT27 — R3012 0 (DNI)

(19) PKT_ERROR4 — RN3012 0
(19) PKT_ERROR5
(19) PKT_VALID0
(19) PKT_VALID1

(19) PKT_VALID2 — RN3013 0
(19) PKT_VALID3
(19) PKT_VALID4
(19) PKT_VALID5

BCM7405

(11,19) GP_PKT_CLK5
(11,19) GP_PKT_DATA5
(11,19) GP_PKT_SYNC5

RN3007 0 (DNI)

RN3014 0 (DNI)

R3013 0

BCM7405
Digital Video Input

GP_VI_656_D0 (10)
GP_VI_656_D1 (10)
GP_VI_656_D2 (10)
GP_VI_656_D3 (10)
GP_VI_656_D4 (10)
GP_VI_656_D5 (10)
GP_VI_656_D6 (10)
GP_VI_656_D7 (10)
GP_VI_656_CLK (10)

Place all the above resistors and rpacks next to BCM740X to minimize stub.

U100-3
BCM7405A1
bga976_35x35_1mm_dp_skt
Digital Video Output

VO_656_0 / LED_LD_0 / EXT_GFX_00	AN33	RN3021	33
VO_656_1 / LED_LD_1 / EXT_GFX_01	AN34		
VO_656_2 / LED_LD_2 / EXT_GFX_02	AM33		
VO_656_3 / LED_LD_3 / EXT_GFX_03	AM34		
VO_656_4 / LED_LD_4 / EXT_GFX_04	AL32		
VO_656_5 / LED_LD_5 / EXT_GFX_05	AL33		
VO_656_6 / LED_LD_6 / EXT_GFX_06	AL34		
VO_656_7 / LED_LD_7 / EXT_GFX_07	AK32		
VO_656_CLK / LED_LS_4 / EXT_GFX_08	AK33	R3021	33

VO_656_D0
VO_656_D1
VO_656_D2
VO_656_D3
VO_656_D4
VO_656_D5
VO_656_D6
VO_656_D7
VO_656_CLK

Strap Bits

VO_656_D0 (13)
VO_656_D1 (13)
VO_656_D2 (13)
VO_656_D3 (13)
VO_656_D4 (13)
VO_656_D5 (13)
VO_656_D6 (13)
VO_656_D7 (13)
VO_656_CLK (13)

Jumper wire. See P9 Rework Instructions.

(10) IRQ10_3510_N

(11,27,28) BSC_M3_SCL
(11,27,28) BSC_M3_SDA
(29) POD_CD2_N — R3014 0 (DNI)

RN3001 0 (DNI)
GP_PKT_CLK5
GP_PKT_DATA5
GP_PKT_SYNC5

RN3002 0 (DNI)
GP_VI_656_D1
GP_VI_656_D7
GP_VI_656_D6

D3.3V D2.5V
C3002 4.7uF
C3003 4.7uF

CCIR-656
VDEC-VEC-AAC-I2S
Daughter Card
Connector

J3001
MICTOR-RCPT-38-VERT.25-HIGH

R3001 33
R3002 33
R3003 33

VI_656_CLK

TP3001

I2S_CLK_IN
I2S_DATA_IN
I2S_LR_IN
EXT_I2S_256FS_CLK
VI_656_D7
VI_656_D6
VI_656_D5
VI_656_D4
VI_656_D3
VI_656_D2
VI_656_D1
VI_656_D0

J3001 pin36 and 38 are connected to active signals on CCIR-656 VDEC-VEC-AAC-I2S daughter card, so they cannot be used for other signals.

Signals come from CCIR-656 VDEC-VEC-AAC-I2S daughter card

Signals go into CCIR-656 VDEC-VEC-AAC-I2S daughter card

D5.0V
C3001 10uF 6.3V

D3.3V
R3004 2.7K

VO_656_CLK

I2S_CLK_OUT
I2S_DATA_OUT
I2S_LR_OUT
AUD_FS_CLK
VO_656_D7
VO_656_D6
VO_656_D5
VO_656_D4
VO_656_D3
VO_656_D2
VO_656_D1
VO_656_D0
IRQ2_TEST_N

AUD_FS_CLK (10)

IRQ2_TEST_N (24)
BCM740X_RST_OUT_N (4,5,17,18,20,21,24,25,27,28,29)

RN3004 33 (DNI)
GP_PKT_SYNC5
GP_PKT_DATA5
GP_PKT_CLK5

RN3005 33
GP_VI_656_D1
GP_VI_656_D7
GP_VI_656_D6

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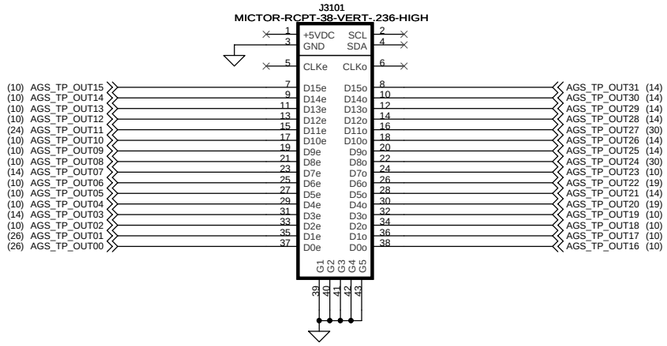

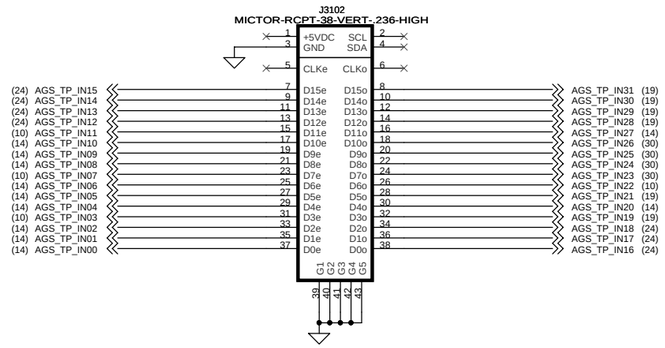

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BCM7405A0 Worst Case Power Measurements (Preliminary - sample of one)

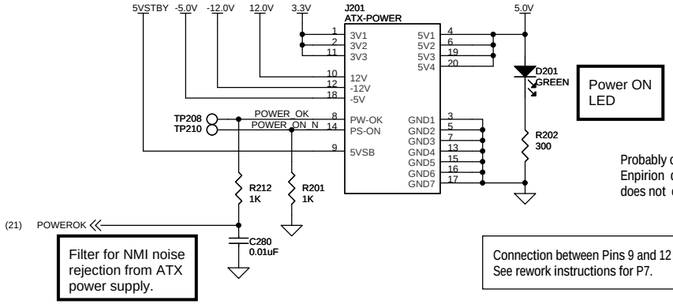
Voltage Rail	Supply (V)	Current (A)	Power (W)
D1.2V_BCM740X	1.2	1.60	1.920
A1.2V_BCM740X	1.2	0.42	0.504
D1.8V_BCM740X	1.8	0.88	1.584
D2.5V_BCM740X	2.5	0.19	0.475
A2.5V_BCM740X	2.5	0.14	0.350
D3.3V_BCM740X	3.3	0.02	0.066
A3.3V_BCM740X	3.3	0.25	0.825
Total Power			5.724

RoHS-compliant ATX Power Supply
BRCM P/N: 533942-00
Vendor: Channel Well Technology
Vendor P/N: PSG300C-D0-GA02-I601-0000FF

P.S. Output

+12V Max 18A, Min 0.3A.
+5V Max 35A, Min 1A.
+5VSB Max 2A, Min 0A.
+3.3V Max 28A, Min 0.3A.
-5V Max 0.5A, Min 0A.
-12V Max 1A, Min 0A.

ATX Power Supply Connector

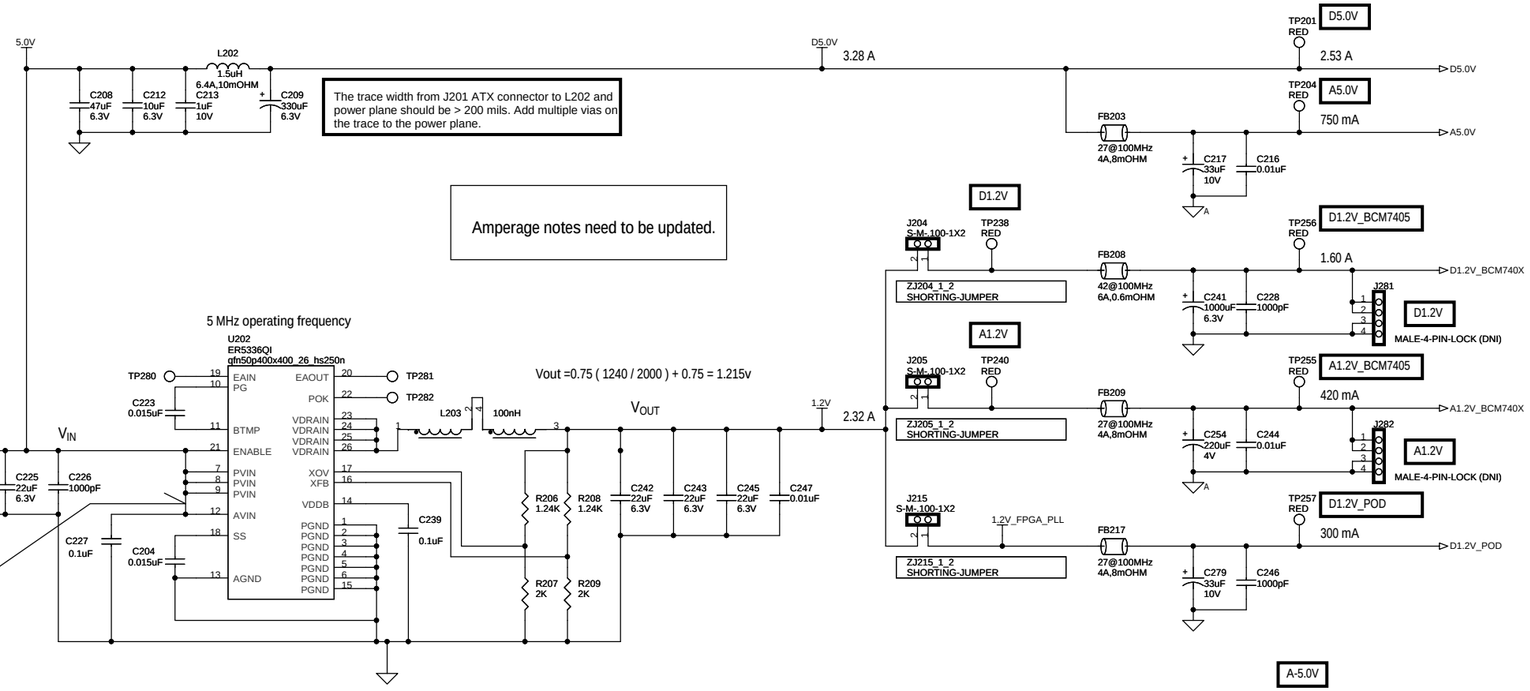


Power ON LED

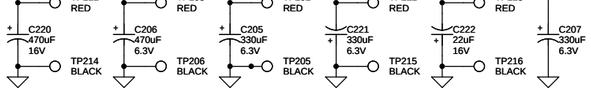
Filter for NMI noise rejection from ATX power supply.

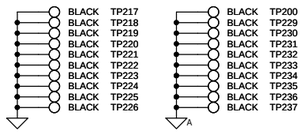
Probably could delete. Enpirion datasheet does not call for it.

Connection between Pins 9 and 12 added by rework. See rework instructions for P7.

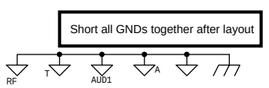


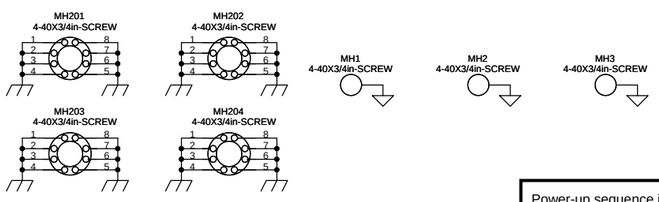
Place these TPs & caps near J201 ATX connector.



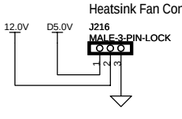


Short all GNDs together after layout

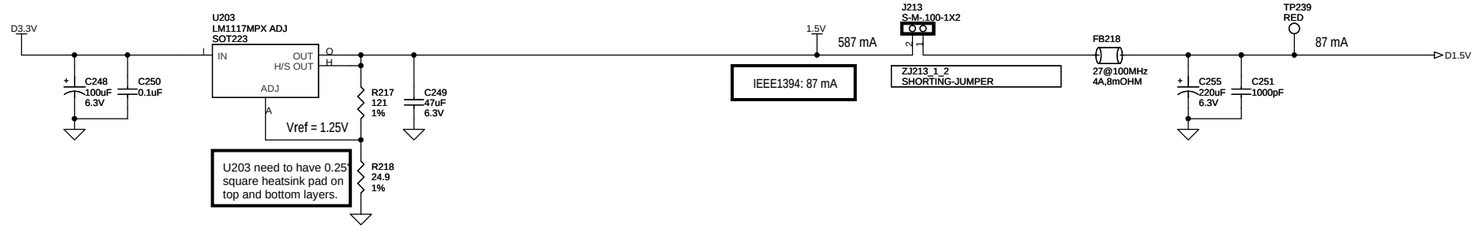




Heatsink Fan Connector



Place J216 near U100.



Power-up sequence is NOT required for Broadcom 65nm chip such as BCM7405. If there are other non-65nm technology based Broadcom chips used on the same board, then the board designer should follow the power-up sequence recommended by those other chips.

Board designer should check carefully and make sure if they need power-up sequence or not when designing the power supply. Inappropriate power sequences may result in chip lock-up, and/or bus contention if other output (to this chip) devices are also driving the signals during power up or down.

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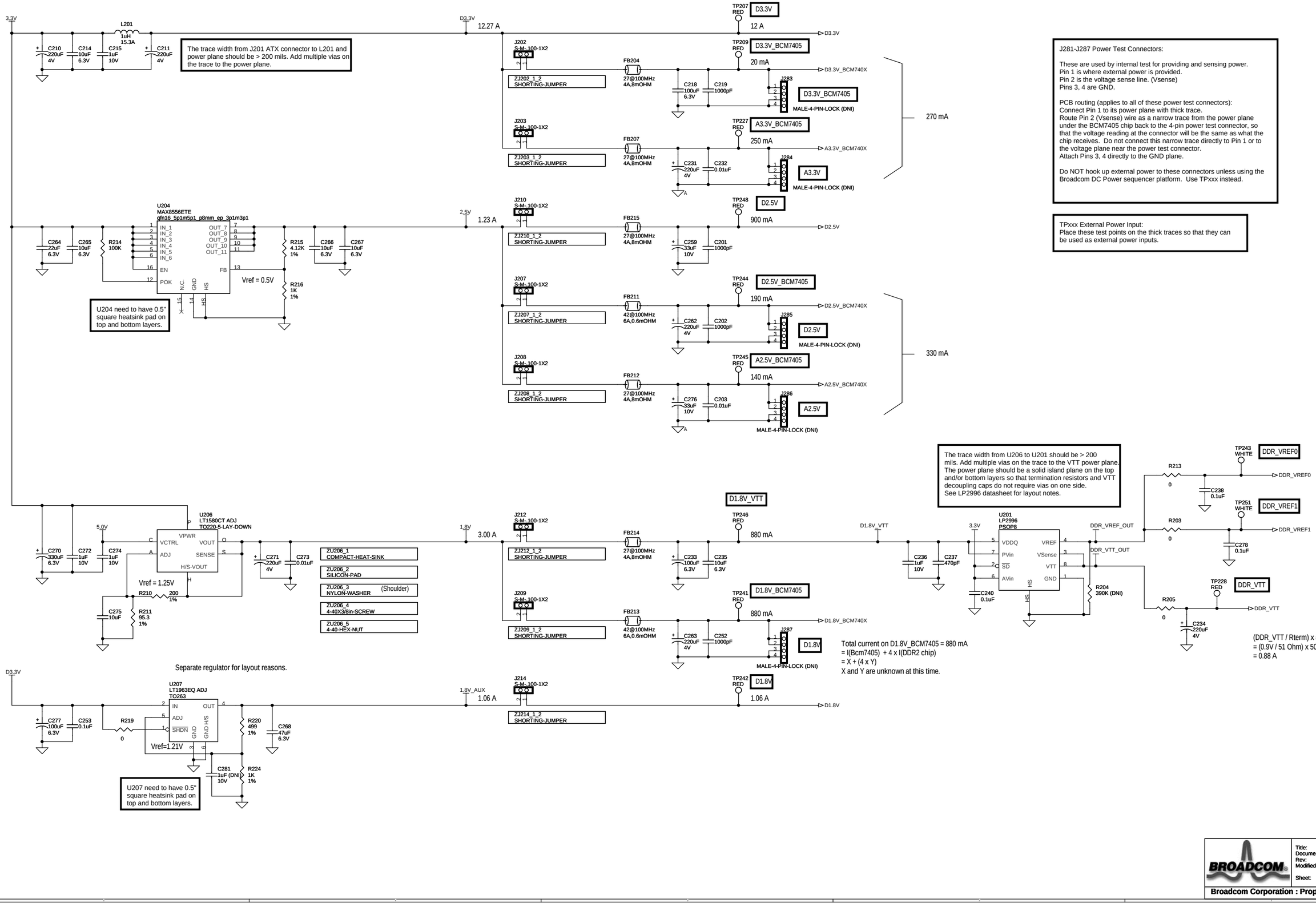
3.3V
L201
1uH
15.3A
C210 220uF 4V
C214 10uF 6.3V
C215 1uF 10V
C211 220uF 4V
The trace width from J201 ATX connector to L201 and power plane should be > 200 mils. Add multiple vias on the trace to the power plane.
D3.3V
12.27 A
TP207 RED
D3.3V
12 A
TP209 RED
D3.3V_BCM7405
20 mA
J202 S-M-100-1X2
ZJ202_1_2 SHORTING-JUMPER
FB204 27@100MHz 4A,8mOHM
C218 100uF 6.3V
C219 1000pF
J283
D3.3V_BCM7405
MALE-4-PIN-LOCK (DNI)
D3.3V_BCM740X
J203 S-M-100-1X2
ZJ203_1_2 SHORTING-JUMPER
FB207 27@100MHz 4A,8mOHM
TP227 RED
A3.3V_BCM7405
250 mA
C231 220uF 4V
C232 0.01uF
J284
A3.3V
MALE-4-PIN-LOCK (DNI)
A3.3V_BCM740X
270 mA
J281-J287 Power Test Connectors:
These are used by internal test for providing and sensing power.
Pin 1 is where external power is provided.
Pin 2 is the voltage sense line. (Vsense)
Pins 3, 4 are GND.
PCB routing (applies to all of these power test connectors):
Connect Pin 1 to its power plane with thick trace.
Route Pin 2 (Vsense) wire as a narrow trace from the power plane under the BCM7405 chip back to the 4-pin power test connector, so that the voltage reading at the connector will be the same as what the chip receives. Do not connect this narrow trace directly to Pin 1 or to the voltage plane near the power test connector.
Attach Pins 3, 4 directly to the GND plane.
Do NOT hook up external power to these connectors unless using the Broadcom DC Power sequencer platform. Use TPxxx instead.
TPxxx External Power Input:
Place these test points on the thick traces so that they can be used as external power inputs.
U204
MAX8556ETE
qfn16_5p1m5p1_p8mm_ep_3p1m3p1
C264 22uF 6.3V
C265 10uF 6.3V
R214 100K
IN_1
IN_2
IN_3
IN_4
IN_5
IN_6
EN
POK
OUT_7
OUT_8
OUT_9
OUT_10
OUT_11
FB
N.C.
GND
HS
Vref = 0.5V
R215 4.12K 1%
R216 1K 1%
C266 10uF 6.3V
C267 10uF 6.3V
U204 need to have 0.5" square heatsink pad on top and bottom layers.
2.5V
1.23 A
J210 S-M-100-1X2
ZJ210_1_2 SHORTING-JUMPER
FB215 27@100MHz 4A,8mOHM
C259 33uF 10V
C201 1000pF
TP248 RED
D2.5V
900 mA
D2.5V
J207 S-M-100-1X2
ZJ207_1_2 SHORTING-JUMPER
FB211 42@100MHz 6A,0.6mOHM
C262 220uF 4V
C202 1000pF
TP244 RED
D2.5V_BCM7405
190 mA
J285
D2.5V
MALE-4-PIN-LOCK (DNI)
D2.5V_BCM740X
J208 S-M-100-1X2
ZJ208_1_2 SHORTING-JUMPER
FB212 27@100MHz 4A,8mOHM
C276 33uF 10V
C203 0.01uF
TP245 RED
A2.5V_BCM7405
140 mA
J286
A2.5V
MALE-4-PIN-LOCK (DNI)
A2.5V_BCM740X
330 mA
The trace width from U206 to U201 should be > 200 mils. Add multiple vias on the trace to the VTT power plane. The power plane should be a solid island plane on the top and/or bottom layers so that termination resistors and VTT decoupling caps do not require vias on one side.
See LP2996 datasheet for layout notes.
U206
LT1580CT ADJ
TO220-5-LAY-DOWN
5.0V
VPWR
VCTRL
VOUT
ADJ
SENSE
H/S-VOUT
Vref = 1.25V
R210 200 1%
R211 95.3 1%
C270 330uF 6.3V
C272 1uF 10V
C274 1uF 10V
C275 10uF
C271 220uF 4V
C273 0.01uF
ZU206_1 COMPACT-HEAT-SINK
ZU206_2 SILICON-PAD
ZU206_3 NYLON-WASHER (Shoulder)
ZU206_4 4-40X3/8in-SCREW
ZU206_5 4-40-HEX-NUT
1.8V
3.00 A
J212 S-M-100-1X2
ZJ212_1_2 SHORTING-JUMPER
FB214 27@100MHz 4A,8mOHM
C233 100uF 6.3V
C235 10uF 6.3V
TP246 RED
D1.8V_VTT
880 mA
D1.8V_VTT
J209 S-M-100-1X2
ZJ209_1_2 SHORTING-JUMPER
FB213 42@100MHz 6A,0.6mOHM
C263 220uF 4V
C252 1000pF
TP241 RED
D1.8V_BCM7405
880 mA
J287
D1.8V
MALE-4-PIN-LOCK (DNI)
D1.8V_BCM740X
C236 1uF 10V
C237 470pF
U201
LP2996
PSOP8
3.3V
VDDQ
PVin
SD
AVin
VREF
VSense
VTT
GND
HS
C240 0.1uF
DDR_VREF_OUT
DDR_VTT_OUT
R204 390K (DNI)
R213 0
C238 0.1uF
TP243 WHITE
DDR_VREF0
R203 0
C278 0.1uF
TP251 WHITE
DDR_VREF1
R205 0
C234 220uF 4V
TP228 RED
DDR_VTT
(DDR_VTT / Rterm) x # of resistors
= (0.9V / 51 Ohm) x 50
= 0.88 A
Total current on D1.8V_BCM7405 = 880 mA
= I(Bcm7405) + 4 x I(DDR2 chip)
= X + (4 x Y)
X and Y are unknown at this time.
Separate regulator for layout reasons.
D3.3V
U207
LT1963EQ ADJ
TO263
IN
OUT
ADJ
SHDN
GND
GND H/S
Vref=1.21V
C277 100uF 6.3V
C253 0.1uF
R219 0
R220 499 1%
C268 47uF 6.3V
C281 1uF (DNI) 10V
R224 1K 1%
U207 need to have 0.5" square heatsink pad on top and bottom layers.
1.8V_AUX
1.06 A
J214 S-M-100-1X2
ZJ214_1_2 SHORTING-JUMPER
TP242 RED
D1.8V
1.06 A
D1.8V
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Size:
Broadcom Corporation : Proprietary and Confidential

A3.3V_BCM740X A2.5V_BCM740X A1.2V_BCM740X

Place all of the power supply filter networks near BCM740X.

U100-11
BCM7405A1
pga976_35x35_1mm_dp_skt

VDAC_AVDD33

R101 0 — UHF_AVDD33 — C31 UHF_AVDD33
R102 0 (DNI) — UHF_AVDD25 — D31 UHF_AVDD25
R103 0 — UHF_AVDD12 — B31 UHF_AVDD12
FB117 600@100MHz 200mA,500mOHM — VDAC_AVDD33 — C26 VDAC0_AVDD33 — D26 VDAC1_AVDD33
R105 0 — VDAC_AVDD25 — D23 VDAC_AVDD25_0 — C23 VDAC_AVDD25_1
R106 0 — VDAC_DVDD12 — C24 VDAC_AVDD12

Use internal voltage regulator by default

C101 DNI, C102 10uF 6.3V, C103 10uF 6.3V, C104 4.7uF, C113 0.1uF, C146 1000pF, C105 DNI, C106 DNI

UHF_AVSS_0 R30, UHF_AVSS_1 C30, UHF_AVSS_2 D29, UHF_AVSS_3 E29, UHF_AVSS_4 E30, UHF_LNA_GND C29, UHF_PLL_GND D30

FB120 600@100MHz — FB118 600@100MHz

VDAC_AVSS_0 E26, VDAC_AVSS_1 E24, VDAC_AVSS_2 E25

R113 0 — HDMI_AVDD33 — D18 HDMI_AVDD33
R109 0 — HDMI_AVDD25 — D19 HDMI_AVDD25
R108 0 — HDMI_AVDD12 — C18 HDMI_AVDD12
FB111 600@100MHz 200mA,500mOHM — HDMI_PLL_VDD12 — C19 HDMI_PLL_VDD12

HDMI_AVSS_0 E17

R111 0 — RFM_AVDD2P5 — C27 RFM_AVDD2P5_0 — C28 RFM_AVDD2P5_1
R112 0 — RFM_AVDD1P2 — D27 RFM_AVDD1P2
R115 0 (DNI) — RFM_PLLCAP — B29 RFM_PLLCAP
R110 0 — AUD0_VDDO25 — D21 AUD0_VDDO25_0
R128 0 — AUD1_VDDO25 — D22 AUD0_VDDO25_1

Use internal voltage regulator by default
(Typical: 8mA, Max: 11mA)
(Typical: 8mA, Max: 11mA)

C160 DNI, C109 DNI, C115 DNI, C138 4.7uF, C110 0.1uF, C111 DNI, C112 DNI, C114 10uF 6.3V, C108 10uF 6.3V, C128 0.1uF, C100 0.01uF, C140 10uF 6.3V, C141 0.1uF, C107 0.01uF

C114 not needed. RFM_PLLCAP now a test port as of 7405B0.

RFM_AVSS_0 E28, RFM_AVSS_1 D28, RFM_AVSS_2 E27

AUD0_VSSO_0 E22, AUD0_VSSO_1 C22, AUD0_VSSO_2 E21

R117 0 — DDR0_BVDD12_0 — AL6 DDR_BVDD0
R119 0 — DDR0_BVDD12_1 — C6 DDR_BVDD1

DDR_BVSS0 AK6, DDR_BVSS1 D7

FB112 600@100MHz 200mA,500mOHM — USB_PLLVDD12 — C12 USB_PLLVDD12
R121 0 — USB_AVDD33 — D13 USB_AVDD33_0 — C13 USB_AVDD33_1
R122 0 — USB_AVDD25 — C11 USB_AVDD25_0
R123 0 — USB_AVDD12 — D10 USB_AVDD12_0 — D11 USB_AVDD12_1
FB115 600@100MHz 200mA,500mOHM — EPHY_AVDD12 — C15 EPHY_AVDD12_0 — D15 EPHY_AVDD12_1
FB113 600@100MHz 200mA,500mOHM — EPHY_BIAS_VDD25 — D16 EPHY_BIAS_VDD25
R104 0 (DNI) — EPHY_PLLVDD12 — D14 EPHY_PLLVDD12 (NOT USED)

C116 0.1uF, C118 0.1uF, C136 4.7uF, C119 0.1uF, C120 DNI, C121 DNI, C122 DNI, C123 4.7uF, C125 0.1uF, C137 4.7uF, C124 0.1uF, C127 4.7uF (DNI), C143 0.1uF (DNI)

USB_AVSS_0 E12, USB_AVSS_1 E11, USB_AVSS_2 E10

EPHY_AVSS_0 E15, EPHY_PLLVSS E16

FB119 120@100MHz 200mA,200mOHM — SATA_AVDD12 — H31 SATA_AVDD12_0 — J30 SATA_AVDD12_1
FB121 120@100MHz 200mA,200mOHM — SATA_PLLVDD12 — J31 SATA_PLLVDD12
R125 0 — CLK54_XVDD25 — D32 CLK54_XVDD25_0 — D33 CLK54_XVDD25_1
R126 0 — XTAL_VDD12 — D34 XTAL_VDD12
FB108 600@100MHz 200mA,500mOHM — PLL_AVDD12 — F32 PLL_AVDD12_0 — G31 PLL_AVDD12_1

C145 4.7uF, C139 0.1uF, C126 4.7uF, C142 0.1uF, C129 0.1uF, C130 0.1uF, C133 4.7uF, C131 0.1uF

SATA_AVSS_0 G32

CLK54_XVSS_0 F31, CLK54_XVSS_1 F30, CLK54_XVSS_2 G30

PLL_AVSS_0 H30

UHF | Video | AUDIO | DDR | USB | ETHERNET | SATA | 3rd OT | SYS PLL | VCXO | HDMI | RFM

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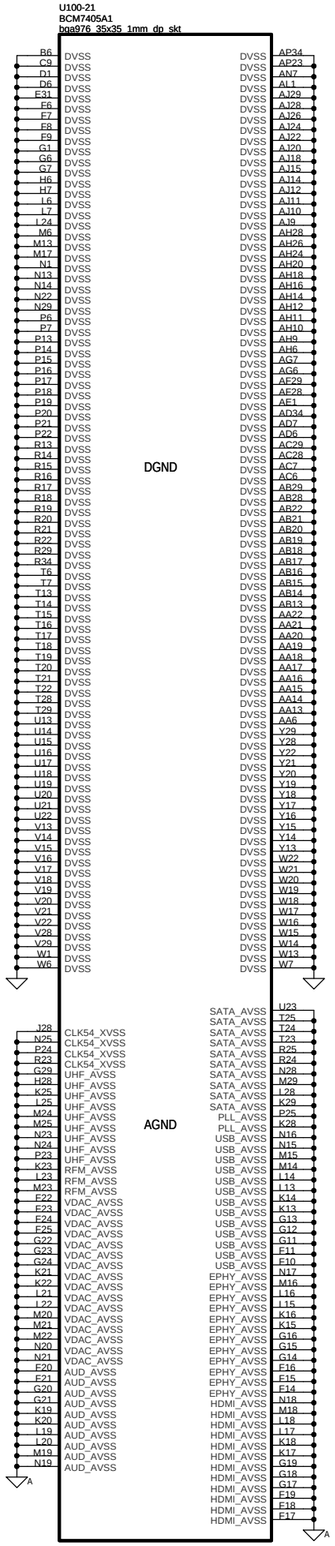
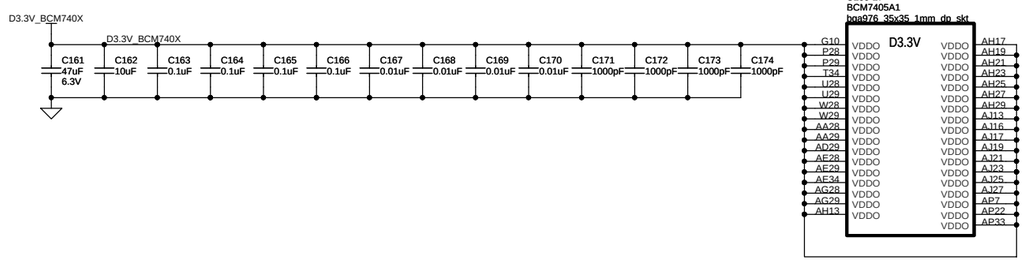
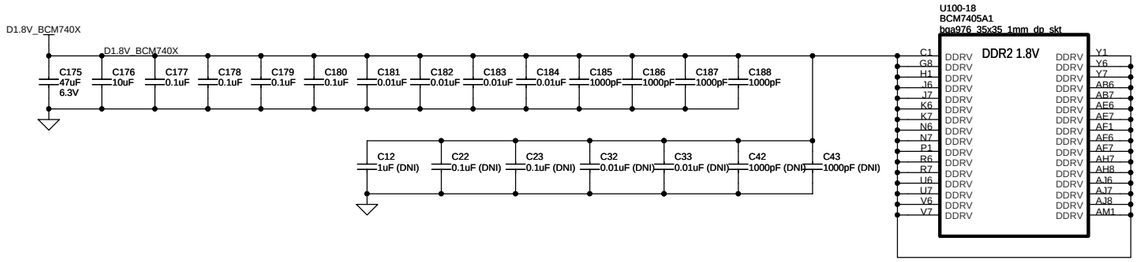


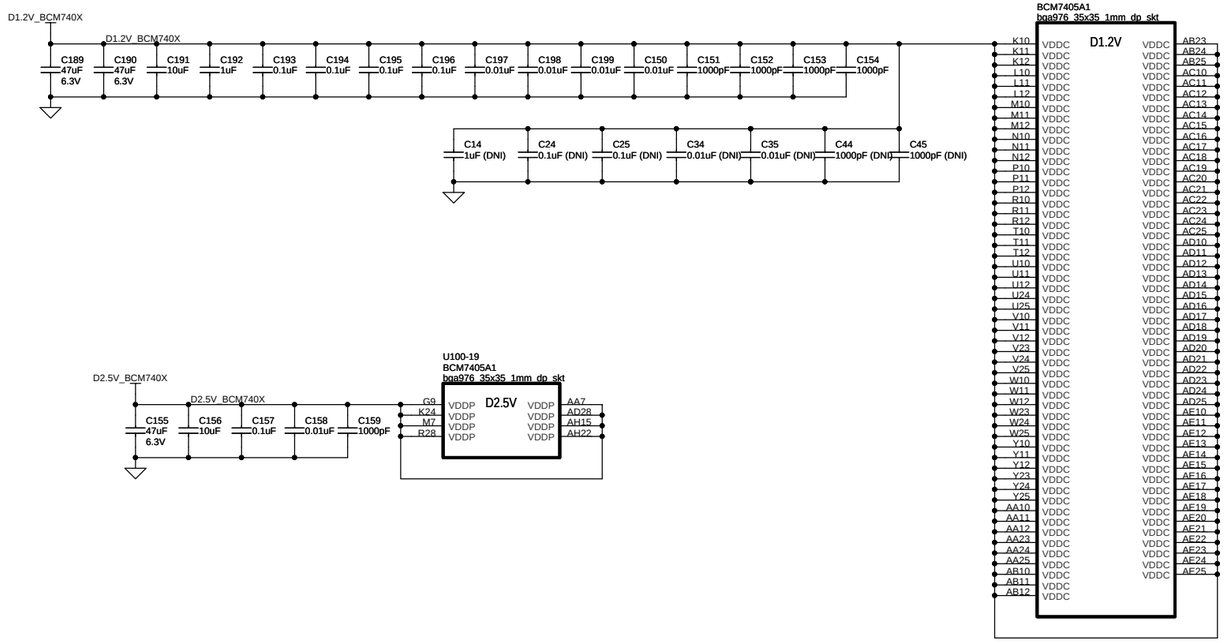
Place all of the decoupling capacitors near BCM740X.

ZU100
HEAT-SINK-35mmSQ-25mmHT

Make corner holes of socket footprint .125" to accommodate heat sink push pins.







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Document: BCM97405MBv00 Schematic
Rev:
Modified: Friday, February 01, 2008

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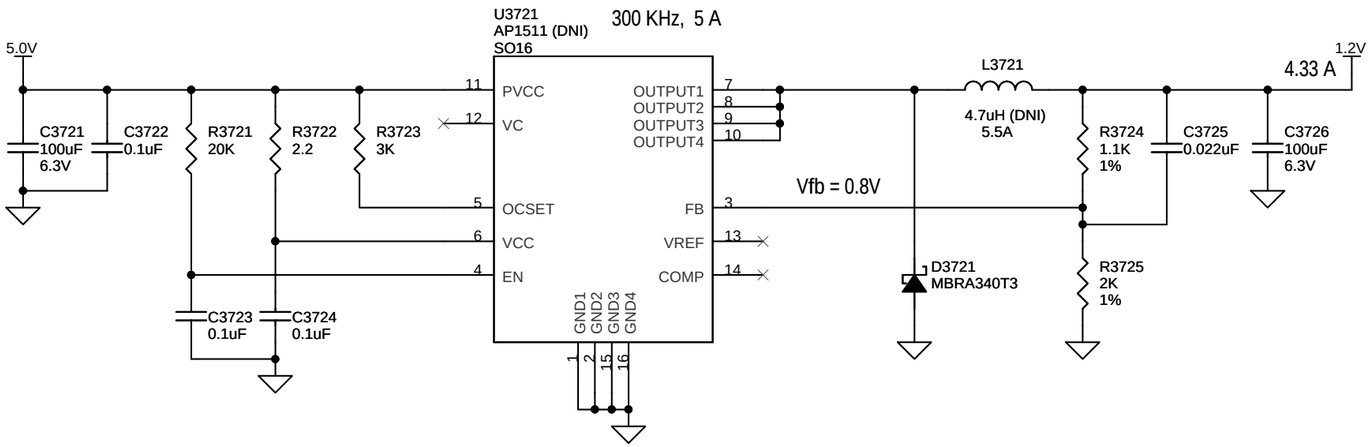
BCM97405MBV00 PCB Stack-up and Impedance Model

PCB Material: FR-4 170 Tg with Er (Dielectric Constant) = 4.3

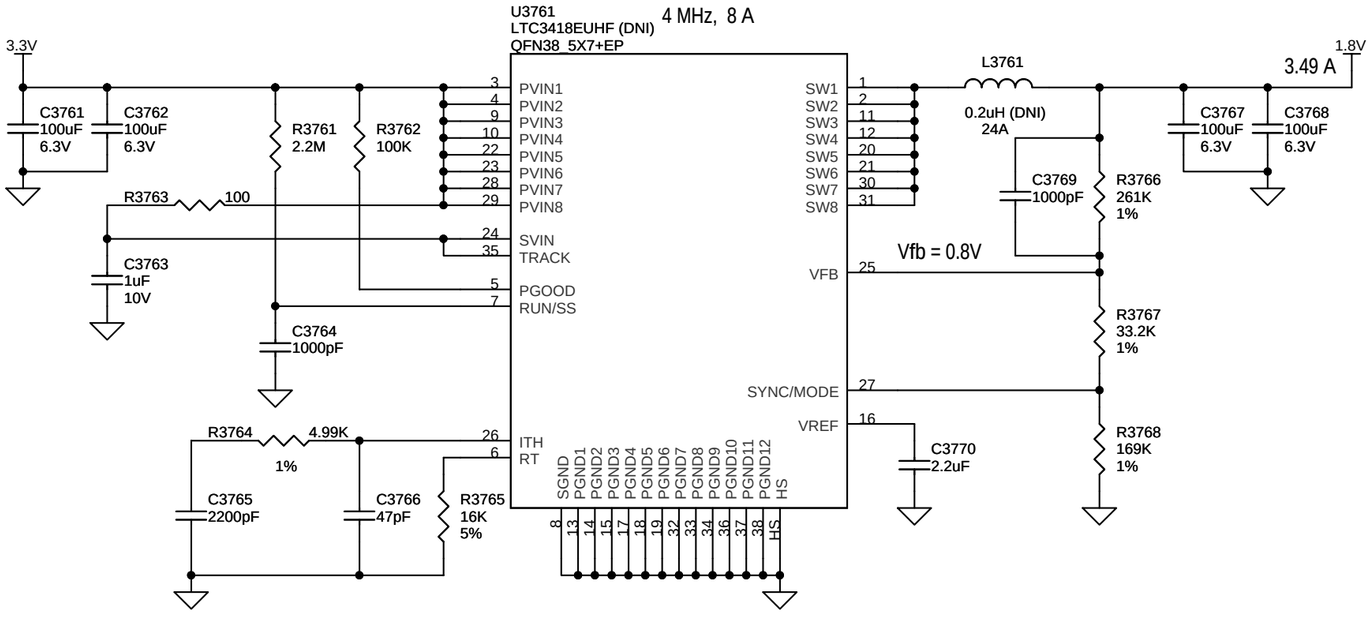
Overall Thickness = 0.078 +/- 10% mils

	Dielectric Thickness (mil)	Layer Definition	Copper (oz)	Target Impedance	Line / Space (mil)	Calculated Impedance	Where used
				50 Ohms +/- 10% differential references to layer 2	7 / 12	50.2 Ohms	DIFF_UHF_IN_P, DIFF_UHF_IN_N
				60 Ohms +/- 10% single-ended	5	59.7 Ohms	DDR_ADDR, DDR_BA, DDR_DQ, DDR_DQM, DDR_RASb, DDR_CASb, DDR_WEb, DDR_CKE, DDR_ODT
				75 Ohms +/- 10% co-planar	5.5 / 12	75.6 Ohms	CH3_4_RF_OUT, VDAC_COMP, VDAC_CHROMA, VDAC_LUMA, VDAC_RED, VDAC_GREEN, VDAC_BLUE
				90 Ohms +/- 10% differential	5.5 / 5.5	90.5 Ohms	DIFF_USBD_P/N
				100 Ohms +/- 10% differential	5 / 7	100.1 Ohms	DDR_DQS/DQSb, DDR_CK/CKb, DIFF_HDMI_P/N, DIFF_HDMI_CLKP/N, DIFF_ENET_TX_P/N, DIFF_ENET_RX_P/N, DIFF_SATA_TX_P/N, DIFF_AUD_RIGHT_P/N, DIFF_AUD0_LEFT_P/N
1		Top Signal	1.5 oz	110 Ohms +/- 10% differential	5 / 11.5	110 Ohms	DIFF_JEDI_TPA0P/N, DIFF_JEDI_TPB0P/N
	5.2			150 Ohms +/- 10% differential references to layer 3	5 / 20	149.8 Ohms	DIFF_RA_I1_P_C/DIFF_RA_I1_N_C, DIFF_RA_Q1_P_C/DIFF_RA_Q1_N_C, RFM_DAC_P/N
2		GND Plane	1.0 oz				
	6.0						
3		Signal	1.0 oz	60 Ohms +/- 10%	5	60.5 Ohms	DDR_ADDR, DDR_BA, DDR_DQ, DDR_DQM, DDR_RASb, DDR_CASb, DDR_WEb, DDR_CKE, DDR_ODT
	46.0						
4		Signal	1.0 oz	60 Ohms +/- 10%	5	60.5 Ohms	
	6.0						
5		Power Plane	1.0 oz				
	5.2						
6		Bottom Signal	1.5 oz	50 Ohms +/- 10% differential references to layer 2	7 / 12	50.2 Ohms	
				60 Ohms +/- 10% single-ended	5	59.7 Ohms	
				75 Ohms +/- 10% co-planar	5.5 / 12	75.6 Ohms	
				90 Ohms +/- 10% differential	5.5 / 5.5	90.5 Ohms	
				100 Ohms +/- 10% differential	5 / 7	100.1 Ohms	
				110 Ohms +/- 10% differential	5 / 11.5	110 Ohms	
				150 Ohms +/- 10% differential references to layer 3	5 / 20	149.8 Ohms	

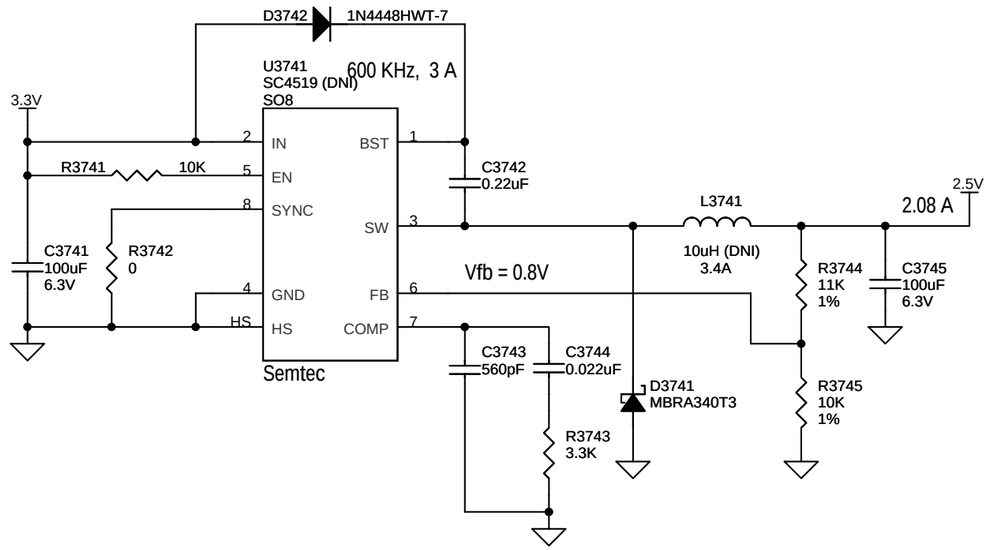
Backup regulator for U202.



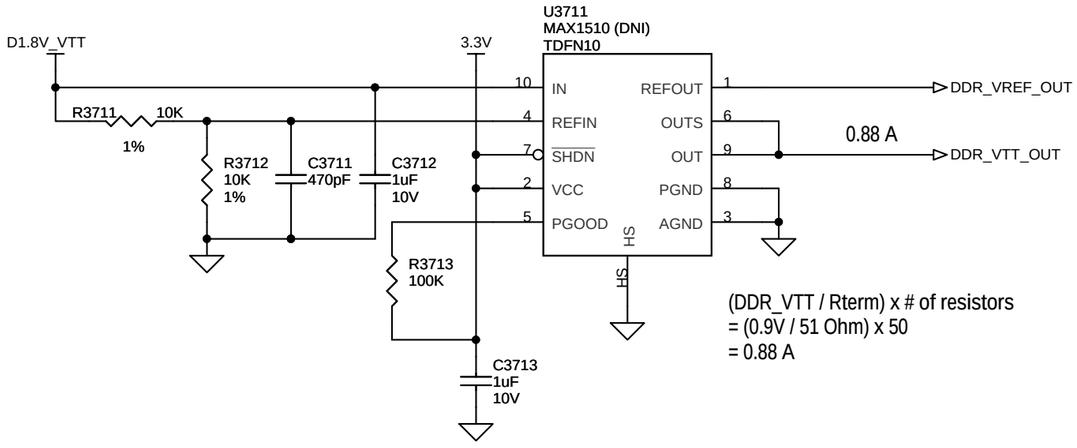
U206 is Backup Regulator for this.



U204 is Backup Regulator for this.



Backup regulator for U201.
2nd source experiment.



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